TOSHIBA

NTDPJTV008

# TECHNICAL TRAINING MANUAL
# N7SS CHASSIS

# PROJECTION TELEVISION

# TP71G90

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# CONTENTS

# SECTION I
# OUTLINE

# 1. OUTLINE

(1) Family common chassis;

TP61G90 (different from TP71G90 in size, data is different from that in contents.)

TW65G80 (WIDE MODEL)

(2) EDTV Engineering;

- Progressive Scan
- Exclusive CRT (long-neck type)—improving Linearity.
- Color-lens employed in R/G (flare reduction )
- New 3D-YCS (common with domestic model, 32DW77)
- Protection sheet (coating) low-refection
- PIP picture-quality is the same as the main pic ture because of using DUAL-UNIT used.

(3) General feature including adjustment are common with TP50G60.

(4) WIDE specifications of TW65G80 are common with TW40F80/TW56F80. (Fig. 1-1)

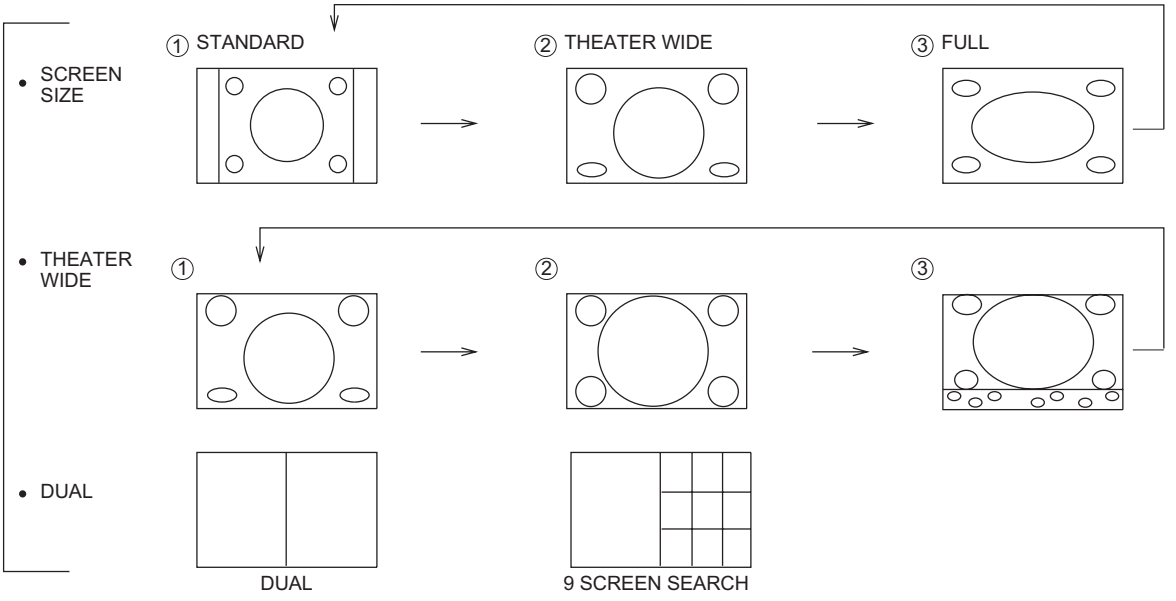



**Fig. 1-1**

# 2. SPECIFICATIONS 37 KEYS

**Table 1-1**

| | Chassis | C - Chassis | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **Model** | TP61G90 | TP61G60 | TP55G90 | TP55G65 | TP55G60 | TP71G90 | TW65G80 | TP50G90 | TP50G60 | TP50G50 | TP48G10 |
| GENER | CRT | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
| | CRT Source | Hitachi | Hitachi | TSB | Hitachi | TSB | Hitachi | Hitachi | Hitachi | Hitachi | Hitachi | Hitachi |
| | Remote H/U | Intell | UnIB/L | Intell | UnIB/L | UnIB/L | Intell | Intell | Intell | UnIB/L | UnIv | UnIv |
| | RMT keys | 37key | 37key | 37key | 37key | 37key | 37key | 37key | 37key | 37key | 38key | 38key |
| | PIP | 2-TN | 2-TN | 2-TN | 2-TN | 2-TN | 2-TN | 2-TN | 2-TN | 2-TN | 1-TN | 1-TN |
| | *V-Chip* | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| SOUND | Dolby Surr | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| | Surround | · | · | · | · | · | · | · | · | · | ¾ | ¾ |
| | SAP | · | · | · | · | · | · | · | · | · | · | · |
| | Cyclone | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| | SBS | · | · | · | · | · | · | · | · | · | · | · |
| | Audio(W) | 28W | 28W | 28W | 28W | 28W | 28W | 28W | 28W | 28W | 28W | 28W |
| | Woofer | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| | Rear | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| PICTURE | Comb-Filter | 3D-Y/C | 2LDIG | 2LDIG | 2LDIG | 2LDIG | 3D-Y/C | 3D-Y/C | 2LDIG | 2LDIG | 2LDIG | 2LDIG |
| | DOF | · | · | · | · | · | · | · | ¾ | ¾ | ¾ | ¾ |
| | Scan-Modul | · | · | · | · | · | · | · | · | · | ¾ | ¾ |
| | VCC | · | · | · | · | · | · | · | · | · | · | · |
| | Black-Expan | · | · | · | · | · | · | · | · | · | · | · |
| | Color-D, E | · | · | · | · | · | · | · | · | · | · | · |
| | Pic-Prefer | · | · | · | · | · | · | · | · | · | · | · |
| | Color-Temp | · | · | · | · | · | · | · | · | · | · | · |
| | Flesh-Tone | · | · | · | · | · | · | · | · | · | · | · |
| | Nois-Reduce | — | · | · | · | · | — | — | · | · | · | · |
| | *Wide Modes* | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | · | ¾ | ¾ | ¾ | ¾ |
| | *Progressive* | · | ¾ | ¾ | ¾ | ¾ | · | · | ¾ | ¾ | ¾ | ¾ |
| | Rori-Resolve | 560DI | 800 | 800 | 800 | 800 | 560DI | 560DI | 800 | 800 | 800 | 800 |
| OTHERS | Fav-Channel | · | · | · | · | · | · | · | · | · | · | · |
| | Ch-label | · | · | · | · | · | · | · | · | · | · | · |
| | 3-Language | · | · | · | · | · | · | · | · | · | · | · |
| | Clock | · | · | · | · | · | · | · | · | · | · | · |
| | Ch-Lock/Off | · | · | · | · | · | · | · | · | · | · | · |
| | C. Caption | · | · | · | · | · | · | · | · | · | · | · |
| | EDS | ¾ | · | · | · | · | ¾ | ¾ | · | · | · | · |
| | New-OSD | · | · | · | · | · | · | · | · | · | ¾ | ¾ |
| | *Multi-Conv* | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| | *D/A Switch* | · | · | · | · | · | · | · | · | · | ¾ | ¾ |
| | *D/W POP* | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | · | ¾ | ¾ | ¾ | ¾ |
| | Multi-Window | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | · | ¾ | ¾ | ¾ | ¾ |
| | S/Sight | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| TERMINAL | S-video In | 1+1 | 1+1 | 1+1 | 1+1 | 1+1 | 1+1 | 1+1 | 1+1 | 1+1 | 1 | 1 |
| | AV-In/Out | 1+2/1 | 1+2/1 | 1+2/1 | 1+2/1 | 1+2/1 | 1+2/1 | 1+2/1 | 1+2/1 | 1+2/1 | 2/1 | 2/1 |
| | *Gold Plated(E2)* | · | · | · | · | · | · | · | · | · | ¾ | ¾ |
| | *Color Differ* | · | · | · | · | · | · | · | · | · | ¾ | ¾ |
| | Front-Term | · | · | · | · | · | · | · | · | · | ¾ | ¾ |
| | A(Var)-OUT | · | · | · | · | · | · | · | · | · | · | · |
| | *AC-3 A.OUT* | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| | 2RF-Term | · | · | · | · | · | · | · | · | · | ¾ | ¾ |
| | SPK-Term | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| | PIP Audio | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| | C-Ch-Input | · | · | · | · | · | · | · | · | ¾ | ¾ | ¾ |
| | E / Jack | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| | S /S-Jack | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| | *RGB (F/R)* | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| ACCE | IR-B & 750 | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| | Adapter | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| | Rod-Antenna | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| | SPK-Box | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ |
| | EZ RMT | ¾ | ¾ | ¾ | ¾ | ¾ | ¾ | *¾ | ¾ | ¾ | ¾ | ¾ |
| | *Protective* | · | OPTION | · | OPTION | OPTION | · | · | · | OPTION | OPTION | OPTION |
| | Cabinet | TP61F80 | TP61F80 | TP55F80 | TP55F80 | TP55F80 | NEW | NEW | TP50F60 | TP50F60 | TP50F50 | TP48F50 |

# 3. TP71G90 SERIES DIFFERENCES

**Table 1-2**

| | | | TP71G90/TP61G90 | TW65G80 |
|---|---|---|---|---|
| SIGNAL | WAC | WAC-UNIT | DEL. | PB6348 |
| | | L518, L519, L520 | DEL. | TEM2028K |
| | | GJ21. GJ22. GJ23 | JP | DEL. |
| | | GJ28 | DEL. | JP |
| | | PW01A. PW02A | DEL. | 8P-BB |
| | WAC-POWER | QQ03. QQ03A. QQ03B | DEL. | PQ09RF11.H/S |
| | | CQ05. CQ06 | DEL. | 50V10 m16V47m |
| | | RQ03 | DEL. | 1/6W4.7K |
| | | QA01 | 8700CSN-113 | 8700CSN-115 |
| | | QA02(MEMORY) | 8K | 16K |
| DEF | D.F.&S.CRRE | SR41 (RELAY) | DEL. | DJ12D1 |
| | | C411 | DEL. | 400V0.027 |
| | | C491 | DEL. | 400V0.15 |
| | | C493 | DEL. | MO.1 |
| | | Q490 | DEL. | 2SC1740S,Q |
| | | Q491 | DEL. | RN1203 |
| | | R498 | DEL. | 4.7K |
| | | D444 | DEL. | 1SS133 |
| | V-SHIFT | C318 | DEL. | MO.1 |
| | | Q304 | DEL. | 2SA1020Y |
| | | Q305 | DEL. | RN1203 |
| | | R321 | DEL. | 2R120 |
| | | R322 | DEL. | 2R120 |
| | | R323 | DEL. | 1/6W1K |
| | | R324 | DEL. | 1/6W5.6K |
| | ABL | R218 | 1/6W10KG | 1/6W12KG |
| | | R220 | 1/6W9.1KG | 1/6W11KG |
| | | R219 | DEL. | 1/6W27KG |
| | | C220 | DEL. | M0.1 |
| | | Q220 | DEL. | RN1204 |

**Table 1-3**

| | | TP71G90 | TP61G90 | TW65G80 | UNIT | BOARD | BASE | BASE UNIT | SPECIFICATION |
|---|---|---|---|---|---|---|---|---|---|
| SIGNAL | PB7289 | O | O | | 23706637 | 23536159 | 23545340 | | E2096K459 |
| | PB7300 | | | O | 23706652 | 23536169 | 23545340 | | E2096K469 |
| DEF | PB7290 | O | O | | 23706638 | 23536160 | 23545341 | | E2096K460 |
| | PB7301 | | | O | 23706653 | 23536170 | 23545341 | | E2096K470 |
| CONV-OUT | PB7291 | O | | | 23706639 | 23536161 | 23545342 | | E2096K461 |
| | PB7396 | | O | | 23706850 | 23536229 | 23545342 | | E2097K003 |
| | PB7302 | | | O | 23706655 | 23536171 | 23545342 | | E2096K471 |
| POWER | PB7292 | O | O | | 23706640 | 23536162 | 23545343 | | E2096K462 |
| | PB7303 | | | O | 23706656 | 23536172 | 23545343 | | E2096K472 |
| A/V | PB7293 | O | O | O | 23706641 | 23536163 | 23545344 | | E2096K463 |
| CRT-FRONT | PB7294 | O | | O | 23706642 | 23536164 | 23545345 | | E2096K464 |
| | PB7571 | | O | | 23781086 | 23526335 | 23545345 | PB7189 | E2097K041 |
| | PB7572 | | O | | 23781091 | 23536336 | 23545296 | | E2097K042 |
| OSD | PB7295 | O | O | O | 23706648 | 23536165 | 23545346 | | E2096K465 |
| | PB7333 | | | | 23706684 | 23536192 | 23545346 | | E2097K001 |
| DIGI-CONV | PB7296 | O | | | 23706649 | 23536166 | 23545347 | | S2096K466 |
| | PB7397 | | O | O | 23706851 | 23536230 | 23545347 | | S2096K004 |
| | PB7304 | | | O | 23706657 | 23536174 | 23545347 | | S2096K473 |
| YCS/DUAL | PB7297 | O | O | O | 23706650 | 23536167 | 23545348 | PB7342 | S2096K467 |
| UP-CON | PB7299 | O | O | O | 23706651 | 23536168 | 23545349 | | S2096K468 |
| WAC | PB6348 | | | | 23705379 | 23535595 | 23484617B | PB5454ZBW | S9095K112 |

# 4. TP71G90 (TW65G80) CHASSIS LAYOUT

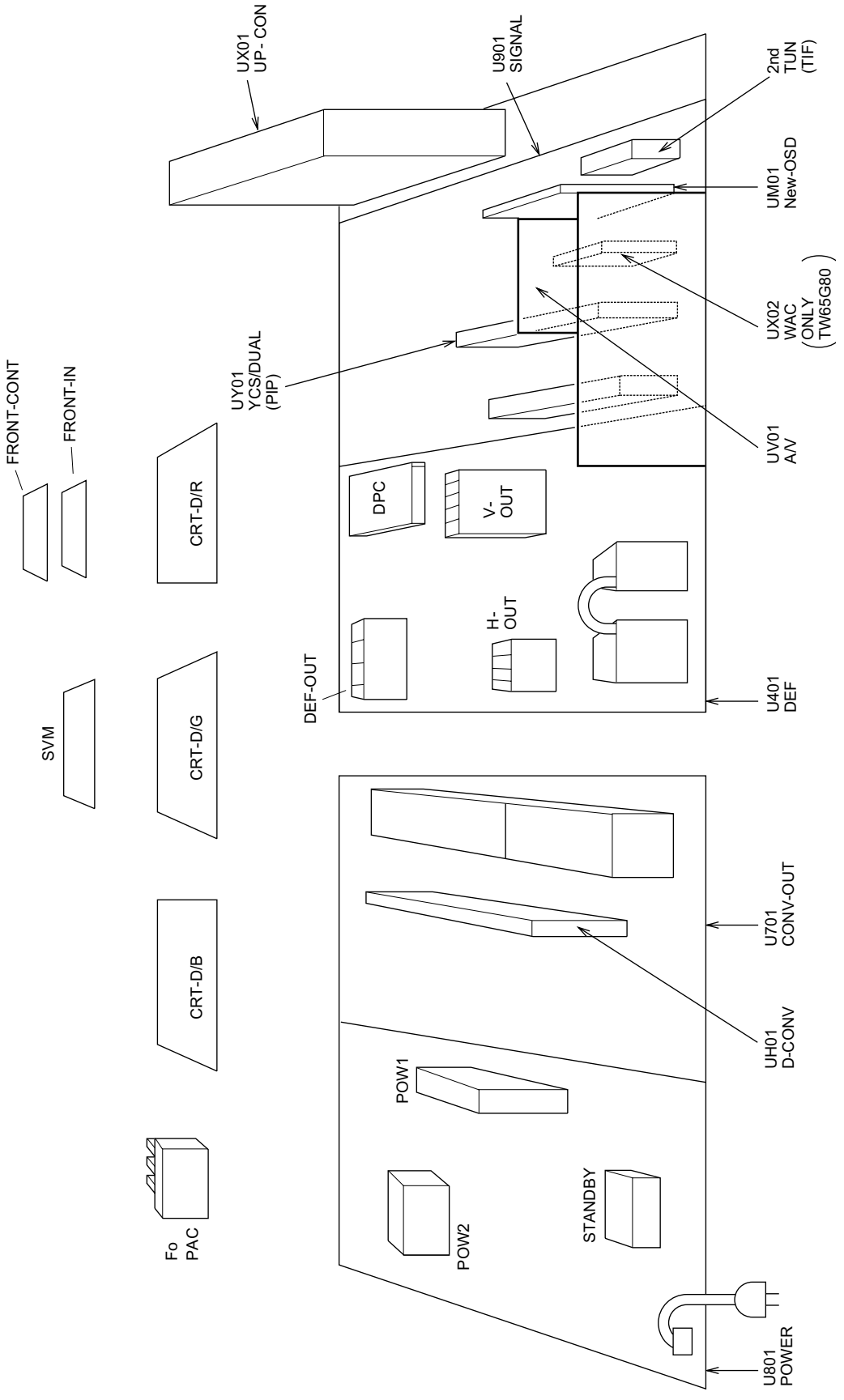



**Fig. 1-2**

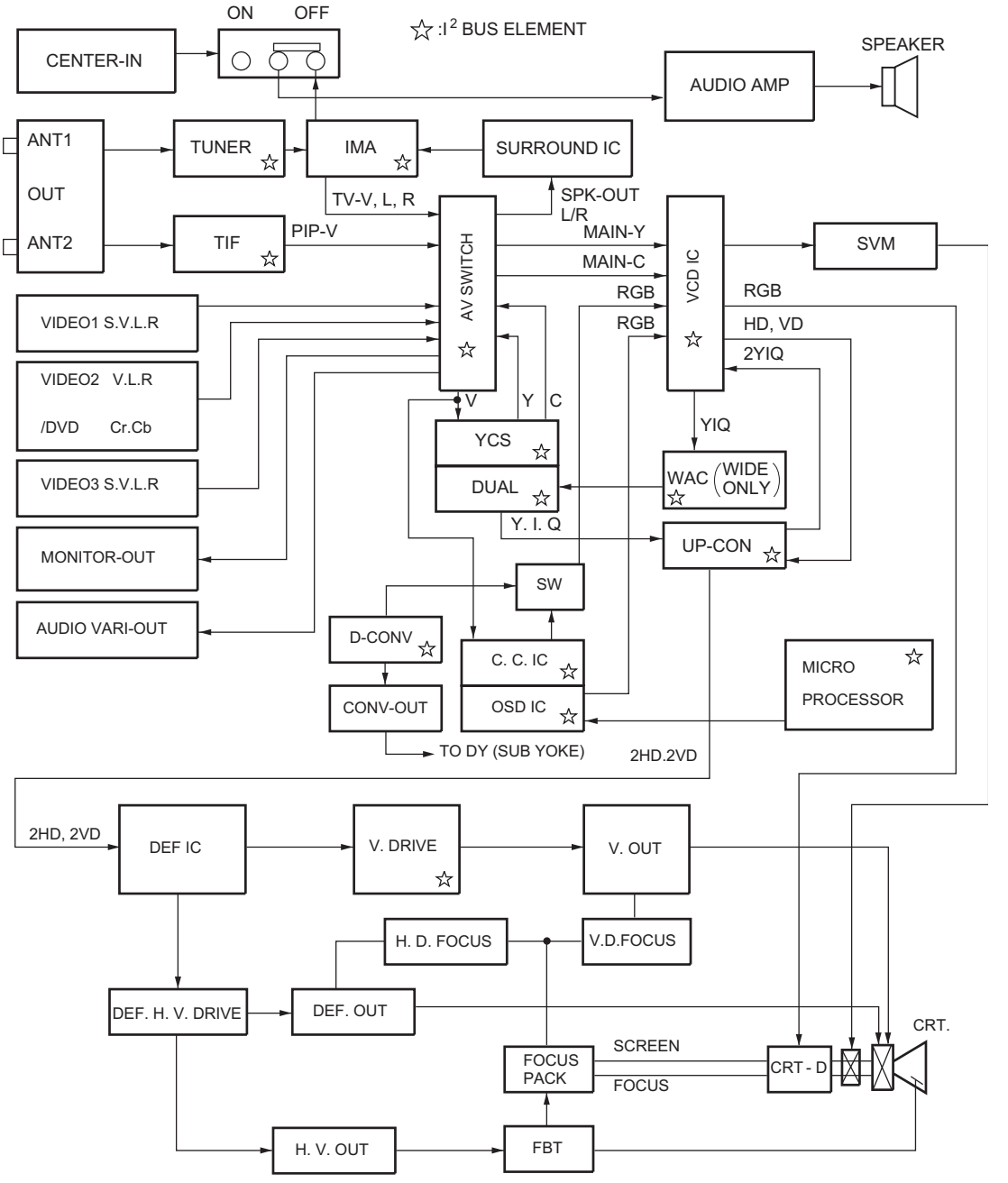



**Fig. 1-3 TP71G90 block diagram**

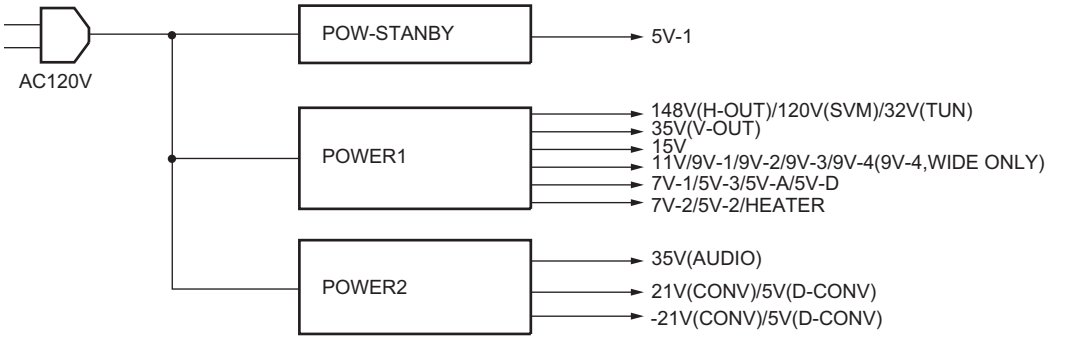



**Fig. 1-4**

# SECTION II
# AUDIO CIRCUIT

# 1. GENERAL

The audio signal processing circuit consists of an input selector IC (QV01 = TA8851CN), a master IMA (H002 = MVUS34S, MVUS34B) modules, a Surround-sound-sound IC (QD01 = TA8173AP) and a VARIABLE-AUDIO-AMP (QS101 = M5218AP) and an audio output IC (Q601 = LA4282). The audio output of TP71G90 is 14W +14W, which is based on SBS (SUB BASS SYSTEM) as a basic specification. When the double window feature is selected, the left-hand screen sound is output.

# 2. FLOW OF SIGNAL

Fig. 2-1 shows a block diagram of the audio circuit of TP71G90.

- TV detection output

  Pins 12 (R-OUT) and 14 (L-OUT) of IMA module H002.

- A/V selector IC input

  Pins 6 (R-IN) and 4 (L-IN) of QV01 (TA8851CN).

  This A/V selector IC receives the audio signals from TV, E1, E2 and E3.

- A/V selector IC output

  Pins 39 (R-OUT) and 41 (L-OUT) of QV01.

  The signal here is regarded as 1.

- Surround-sound-sound IC input

  Pins 16 (R-IN) and 14 (L-IN) of QD01.

- Surround-sound-sound IC output

  Pins 9 (R-OUT) and 11 (L-OUT) of QD01.

- IMA module A. PRO input

  Pins 16 (R-IN) and 18 (L-IN) of H002.

- IMA module A. PRO output

  Pins 26 (R-OUT), 24 (L-OUT) and 22 (W-OUT) of H002.

- VARIABLE-AUDIO-AMP input

  Pins 3 (R-IN) and 5 (L-IN) of QS101.

- VARIABLE-AUDIO-AMP output

  Pins 1 (R-OUT) and 7 (L-OUT) of QS101.

- Audio output IC input

  Pins 2 (R-IN) and 5 (L-IN) of Q601.

- Audio output IC output

  Pins 11 (R-OUT) and 7 (L-OUT) of Q601.

- SPK output

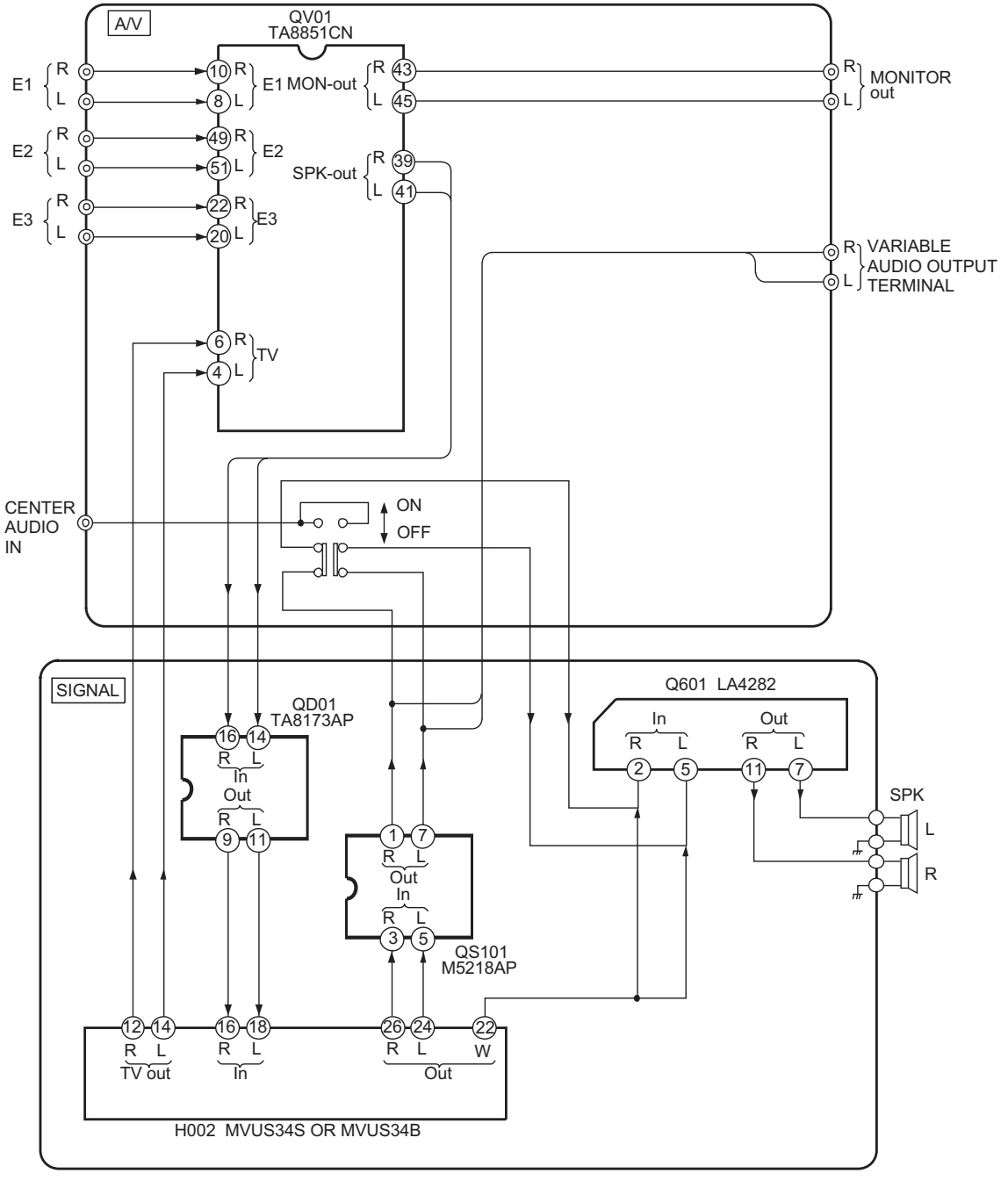



**Fig. 2-1 Audio circuit block diagram**

# 3. DESCRIPTION OF CIRCUITS

## 3-1. IMA Module (MVUS34S/MVUS34B)

### 3-1-1. MTS Circuit

This has the following functions.

- Discriminating STEREO and SAP
- MATRIX output selection for STEREO and SAP

Table 2-1 shows the output MATRIX in each broadcast mode.

**Table 2-1 Multi-channel MATRIX**

| Feed | Mode selection | Speaker output | | Multi-channel display | |
|---|---|---|---|---|---|
| | | L | R | Stereo | SAP |
| MONO | STEREO | MONO | MONO | | |
| | SAP | MONO | MONO | | |
| | MONO | MONO | MONO | | |
| STEREO | STEREO | L | R | O | |
| | SAP | L | R | O | |
| | MONO | L + R | L + R | O | |
| MONO + SAP | STEREO | MONO | MONO | | O |
| | SAP | SAP | SAP | | O |
| | MONO | MONO | MONO | | O |
| STEREO + SAP | STEREO | L | R | O | O |
| | SAP | SAP | SAP | O | O |
| | MONO | L + R | L + R | O | O |

## 3-2. A. PRO Circuit

The self-made A. PRO TA1217AN is used. This has the following functions.

- VOLUME CONTROL
- TONE CONTROL (BASS, TREBLE, BALANCE)
- SBS LEVEL CONTROL
- SBS ON/OFF

All these functions are controlled by $I^2C$ BUS sent from a microcomputer.

Fig. 2-2 shows the block diagram of A. PRO.

## 3-3. A/V Selector Circuit

(1) Input source selected with QV01

Signals from TV, E1, E2 and E3

Fig. 2-3 shows the internal block diagram of QV01 (TA8851CN). Select always the master (left-hand screen) signal for the SPK-OUT (pins 39 and 41) signal.

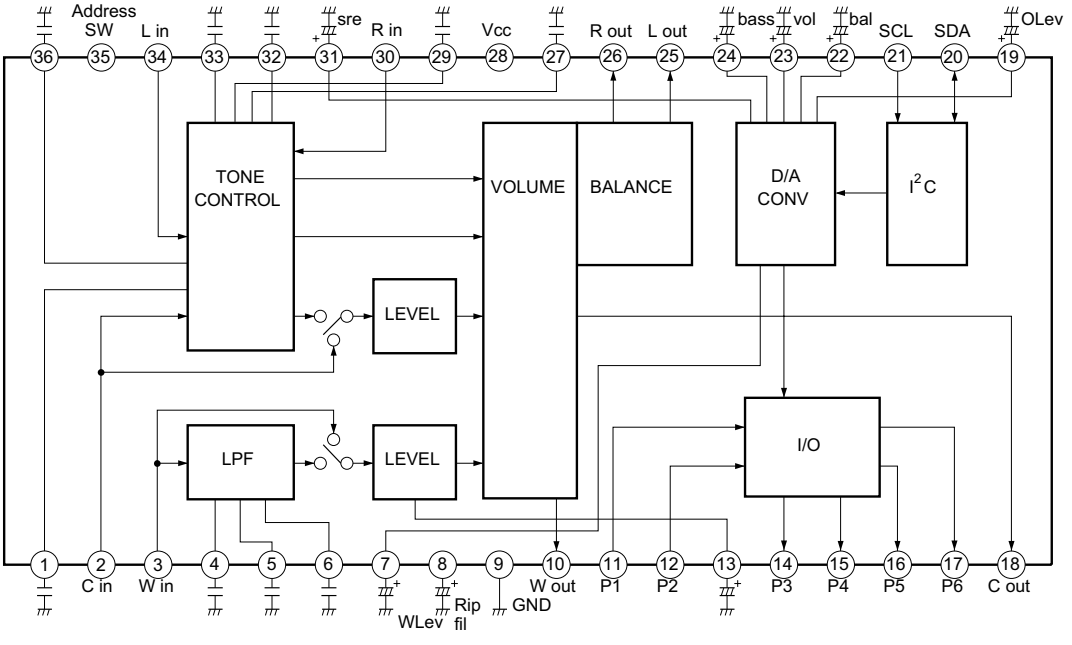



**Fig. 2-2 TA1217AN block diagram**

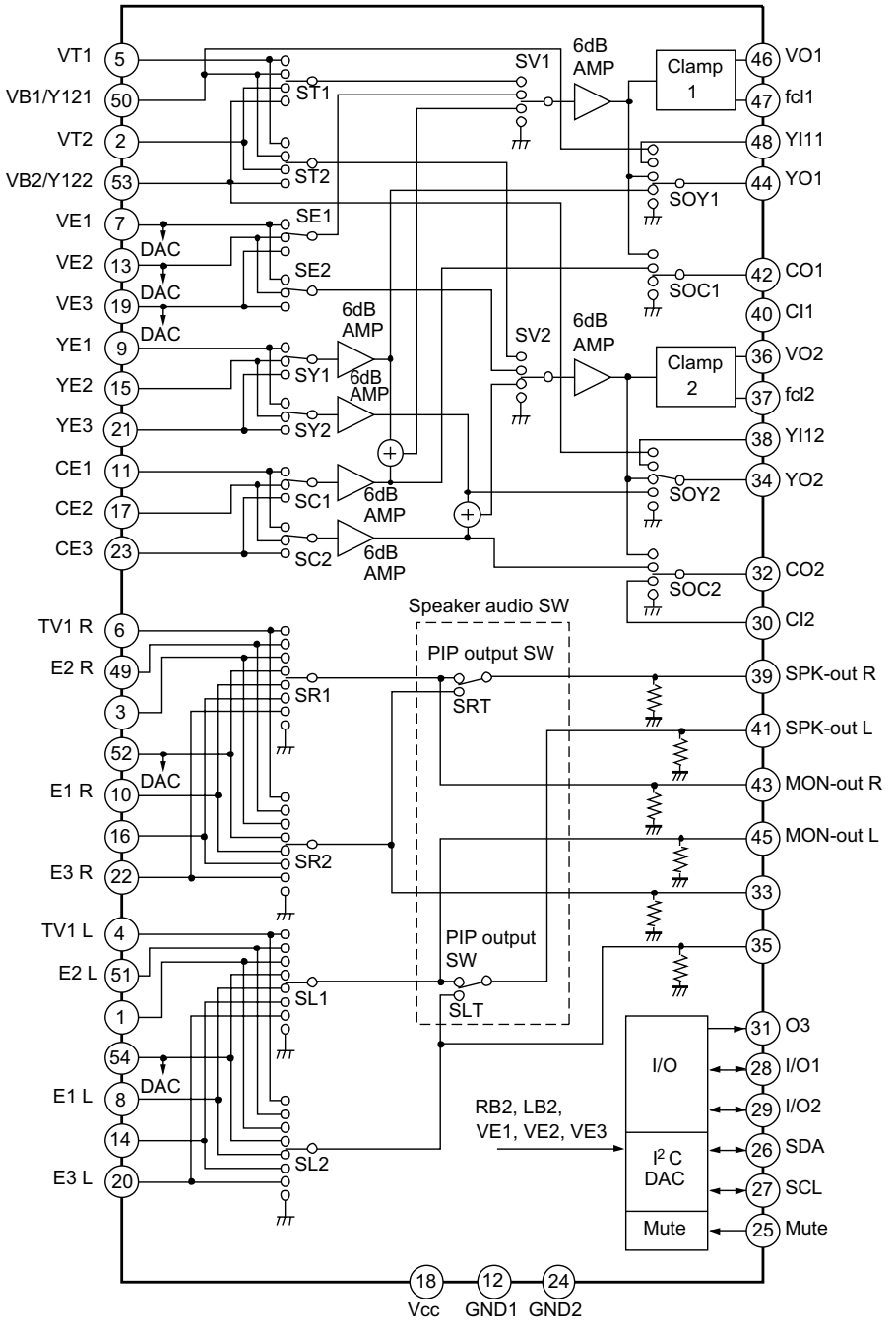



**Fig. 2-3 QV01 (TA8851CN) block diagram**

## 3-4. Surround-sound Circuit

Surround-sound processing is performed by TA8173AP.

Fig. 2-4 shows the internal block diagram of TA8173AP.

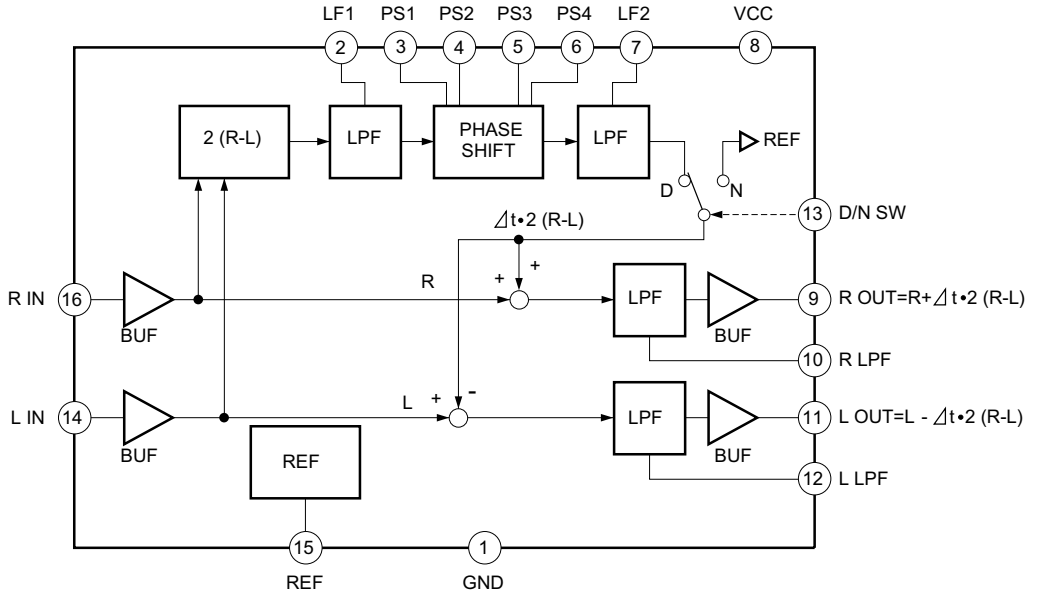



**Fig. 2-4 Surround process IC TA8173AP block diagram**

## 3-5. Audio Output Circuit

This uses LA4282, and permits output of 14W + 14W.

Fig. 2-5 shows the block diagram.

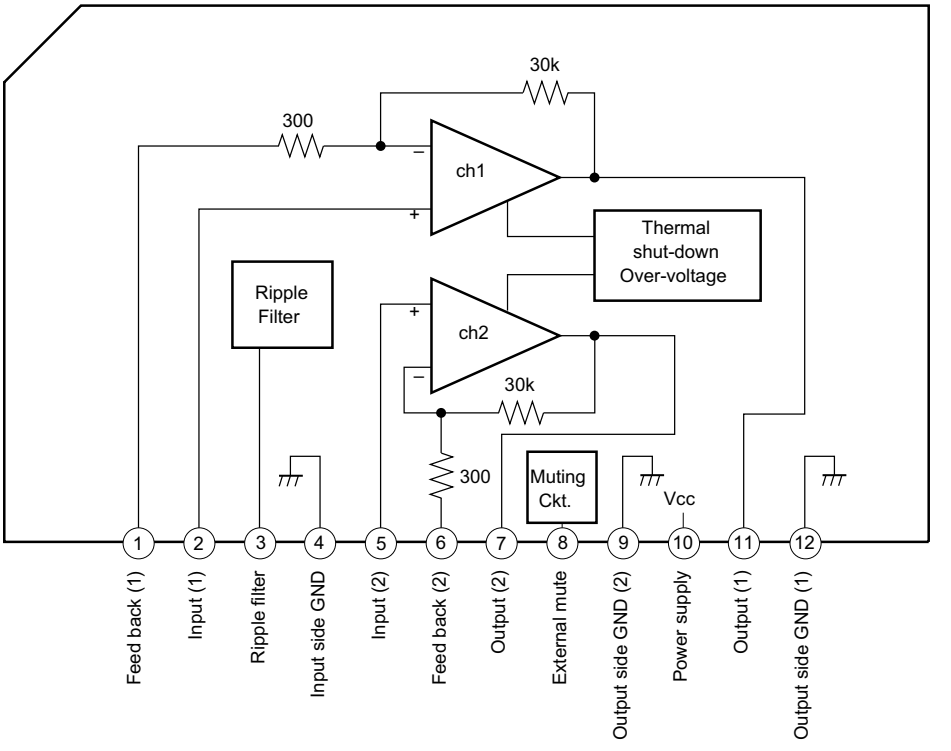



**Fig. 2-5 LA4282 block diagram**

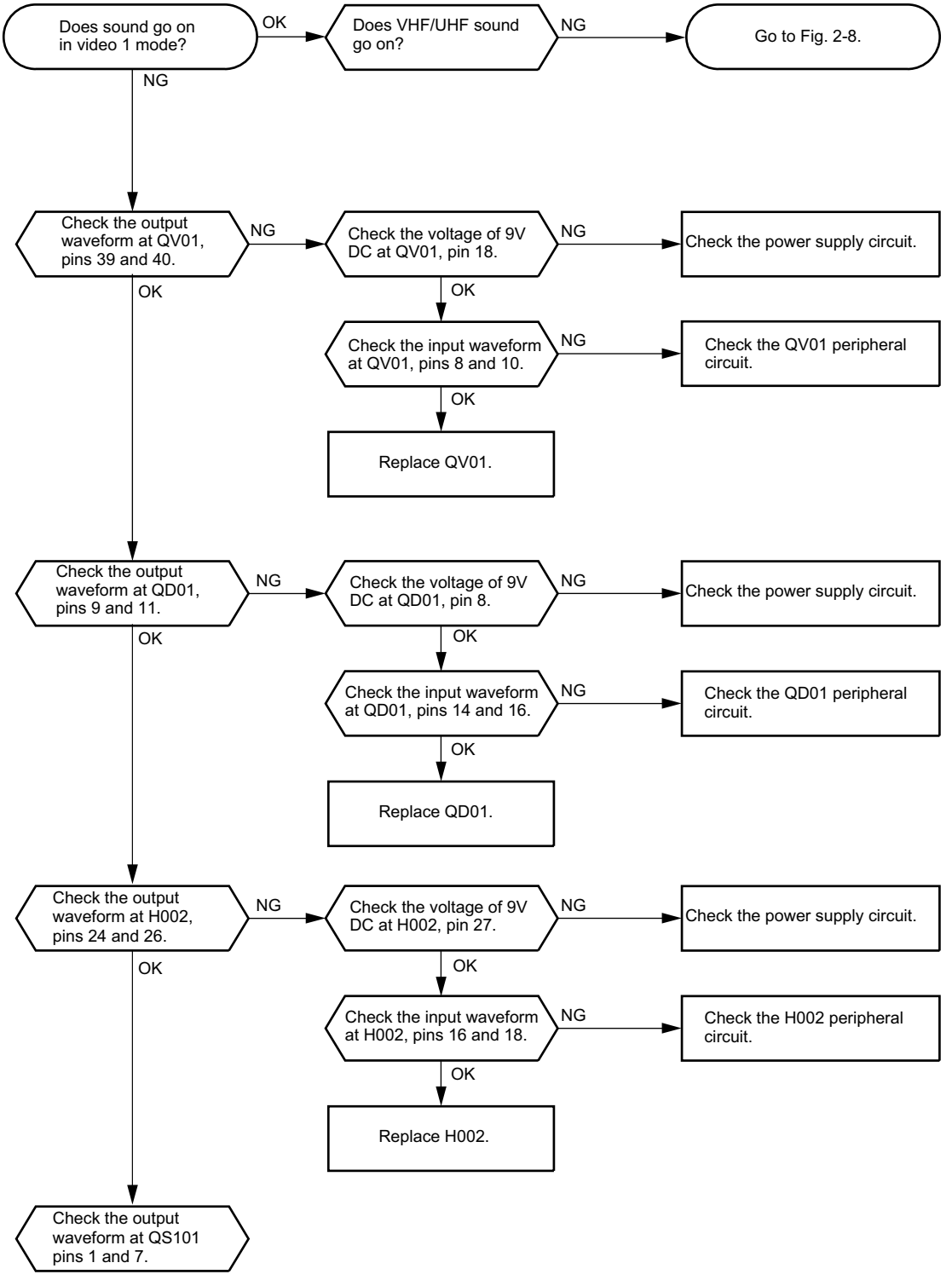

Does sound go on in video 1 mode?
OK
Does VHF/UHF sound go on?
NG
Go to Fig. 2-8.
NG
Check the output waveform at QV01, pins 39 and 40.
NG
Check the voltage of 9V DC at QV01, pin 18.
NG
Check the power supply circuit.
OK
OK
Check the input waveform at QV01, pins 8 and 10.
NG
Check the QV01 peripheral circuit.
OK
Replace QV01.
Check the output waveform at QD01, pins 9 and 11.
NG
Check the voltage of 9V DC at QD01, pin 8.
NG
Check the power supply circuit.
OK
OK
Check the input waveform at QD01, pins 14 and 16.
NG
Check the QD01 peripheral circuit.
OK
Replace QD01.
Check the output waveform at H002, pins 24 and 26.
NG
Check the voltage of 9V DC at H002, pin 27.
NG
Check the power supply circuit.
OK
OK
Check the input waveform at H002, pins 16 and 18.
NG
Check the H002 peripheral circuit.
OK
Replace H002.
Check the output waveform at QS101 pins 1 and 7.

**Fig. 2-6**

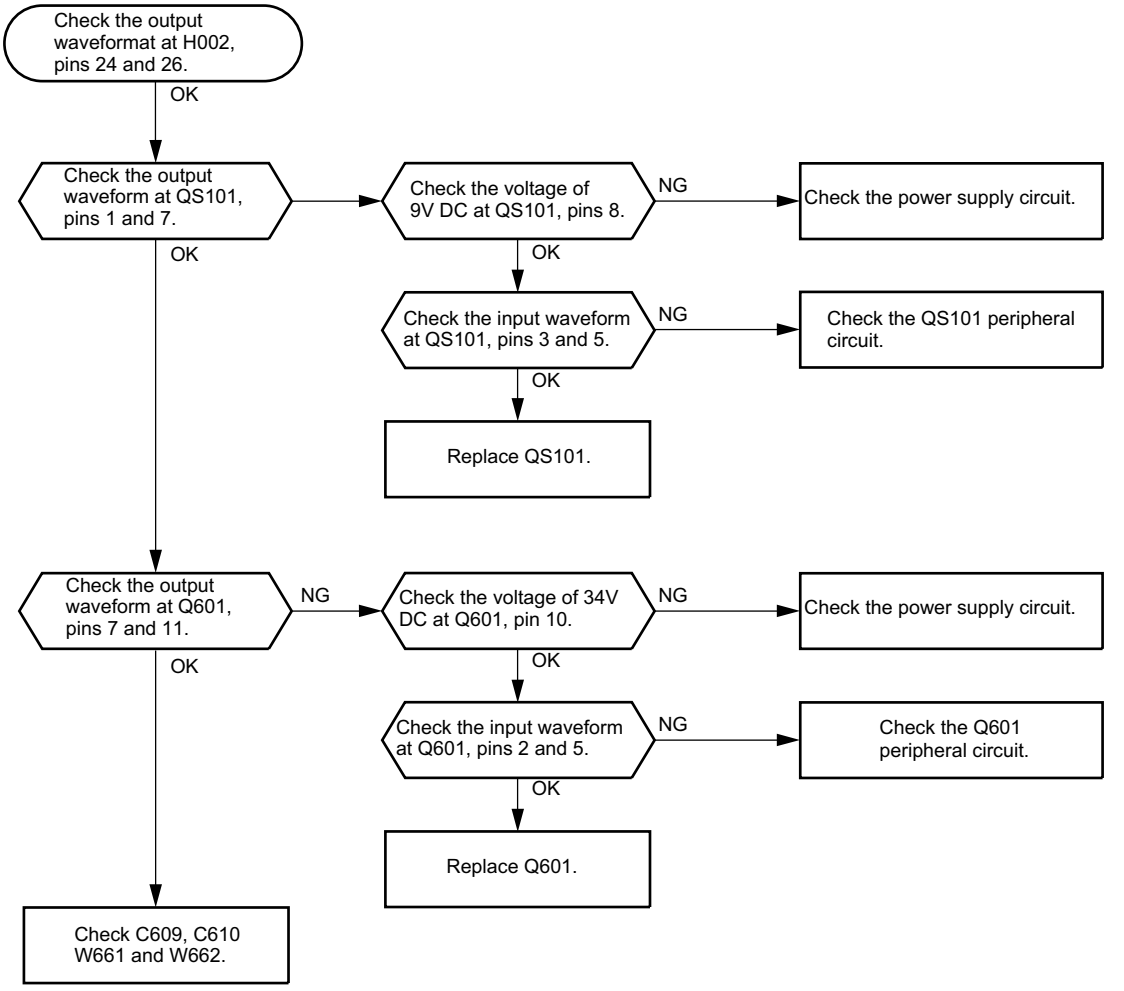

Check the output waveformat at H002, pins 24 and 26.
OK
Check the output waveform at QS101, pins 1 and 7.
Check the voltage of 9V DC at QS101, pins 8.
NG
Check the power supply circuit.
OK
OK
Check the input waveform at QS101, pins 3 and 5.
NG
Check the QS101 peripheral circuit.
OK
Replace QS101.
Check the output waveform at Q601, pins 7 and 11.
NG
Check the voltage of 34V DC at Q601, pin 10.
NG
Check the power supply circuit.
OK
OK
Check the input waveform at Q601, pins 2 and 5.
NG
Check the Q601 peripheral circuit.
OK
Replace Q601.
Check C609, C610 W661 and W662.

**Fig. 2-7**

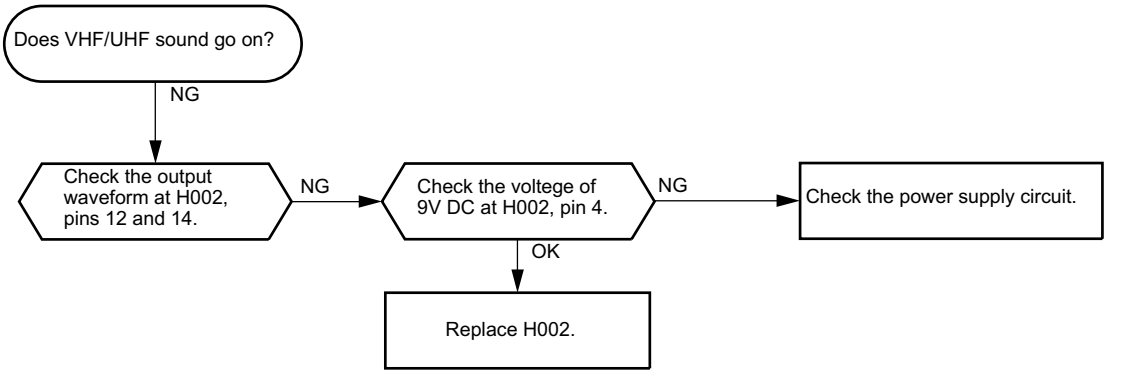

Does VHF/UHF sound go on?
NG
Check the output waveform at H002, pins 12 and 14.
NG
Check the voltege of 9V DC at H002, pin 4.
NG
Check the power supply circuit.
OK
Replace H002.

**Fig. 2-8**

# SECTION III
# TUNER/IMA CIRCUIT

# 1. CIRCUIT BLOCK

## 1-1. Outline

A TV signal input to ANT1 is provided to HY01 (TIF for PIP) and H001 (main tuner) through a splitter H003(RF-SW) is a new RF-SWITCH with an isolation amplifir added to the divider output to improve local interference between the main and the sub tuner.

H003 controls, signal selection for ANT1 or ANT2 to be supplied to H001 (main tuner) according to the IMA MODULE-DAC-OUT 2.

H001 is of an international standardtype tuner and supplies the signals (Video: 45.75 MHz Audio: 41.25 MHz) in the IF (Intermediate-Frequency) band to the IMA.

The TV signal input to ANT1 is always provided to HY01 (TIF for PIP) as the splitter output and demodulated to a video signal for PIP.

H002 (IMA) is module containing the IF circuit consisting of a split carrier PLL synchronizing detection system and multiplex sound decorder and audio processer.

But in the MPX section, former HIC type is replaced by a module consisting of MPX-IC, $I^2C$ bus control and sound multiplex data exclusive memory IC, thereby affering a non alignment in the replacement service.

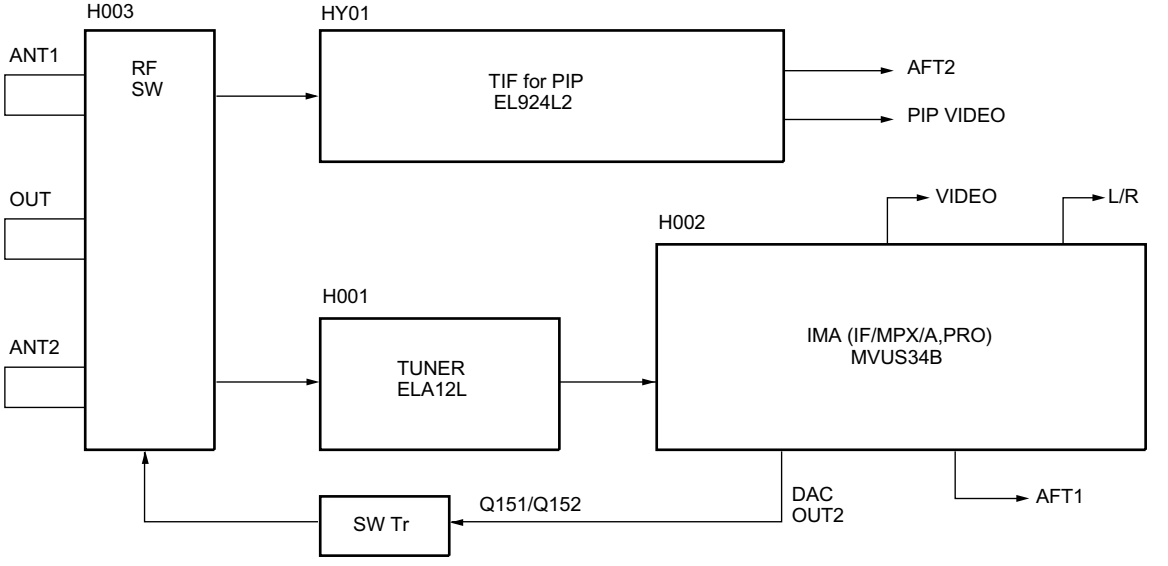



**Fig. 3-1 Block diagram**

## 1-2. RF SW

H003 Model : RSU134 (SN : 23344412)

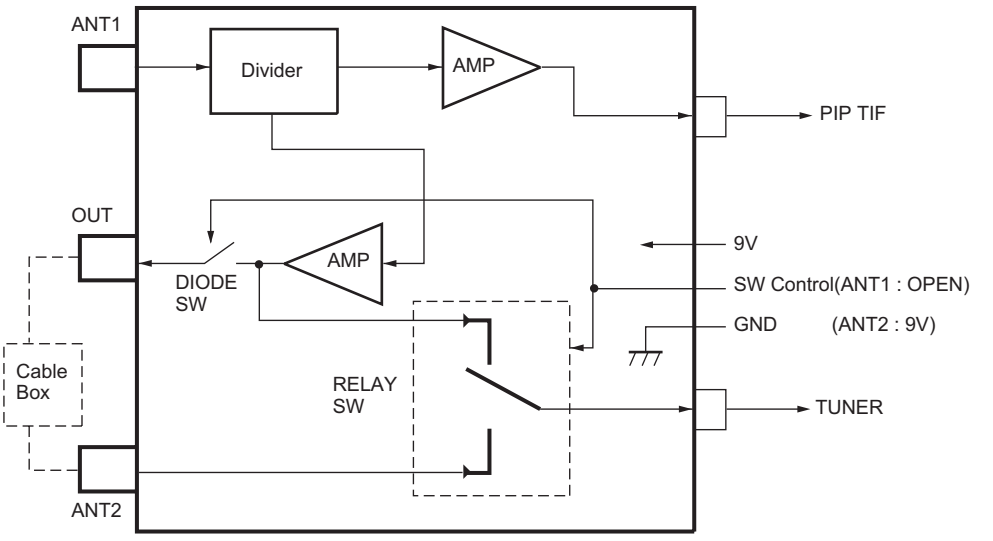
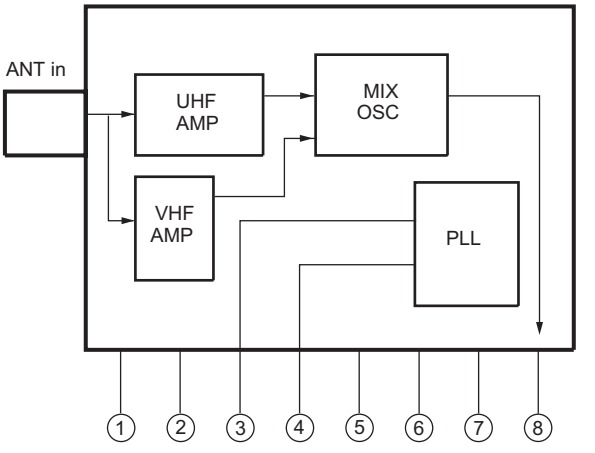



**Fig. 3-2 Block diagram**

## 1-3. TUNER

H001 Model : ELA12L (SN : 23321223)




| Pin No. | Name |
|---|---|
| 1 | AGC |
| 2 | ADDRESS |
| 3 | CLOCK |
| 4 | DATA |
| 5 | 9V |
| 6 | 5V |
| 7 | 32V |
| 8 | IF |

**Fig. 3-3 Block diagram**

Pin2 (ADDRESS) in the main tuner is open and controlled by microcomputer

RECEPTION BAND AREA VHF LOW : CH~2B

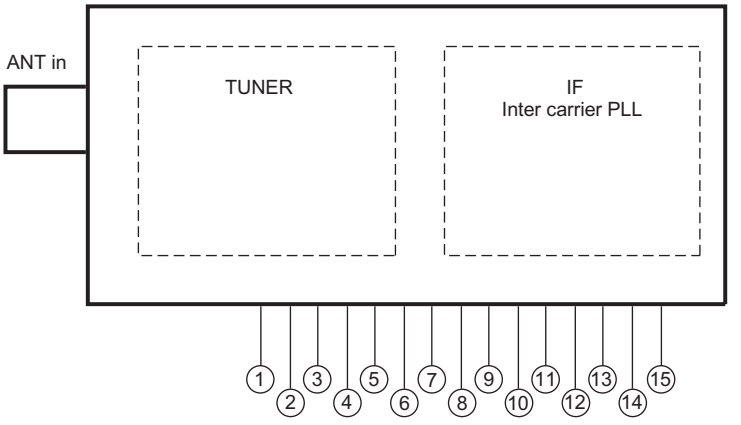
VHF HIGH : CHC~LL

UHF : CHMM~69

## 1-4. TIF for PIP

TIF for PIP with no-sound is newly developed.

HY01 Model : EL924L2 (SN : 23321263)




| Pin No. | Name |
|---|---|
| ① | NC |
| ② | 32V |
| ③ | CLOCK |
| ④ | DATA |
| ⑤ | NC |
| ⑥ | ADDRESS |
| ⑦ | 5V |
| ⑧ | RF AGC |

| Pin No. | Name |
|---|---|
| ⑨ | 9V |
| ⑩ | NC |
| ⑪ | GND |
| ⑫ | AFT |
| ⑬ | NC |
| ⑭ | GND |
| ⑮ | VIDEO |

**Fig. 3-4**

The Pin6 (ADDRESS) in the PIP TIF is GND, and controlled by the microcomputer.

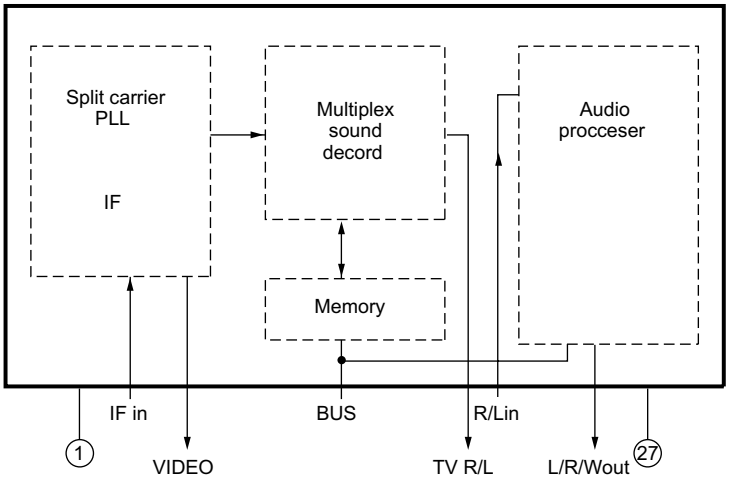
RECEPTION BAND AREA VHF LOW : CH2~B

VHF HIGH : CHC~LL

UHF : CHMM~69

## 1-5. IMA

H002 Model : MVUS34B (SN : 23148280)




| Pin No. | Name |
|---|---|
| ① | GND |
| ② | IF in |
| ③ | NC |
| ④ | 9V |
| ⑤ | RF AGC |
| ⑥ | AFC |
| ⑦ | VIDEO |
| ⑧ | IF AGC |
| ⑨ | MPX out |
| ⑩ | SAP VCO |
| ⑪ | ADDRESS |
| ⑫ | TV R |
| ⑬ | DAC out 1 |

| Pin No. | Name |
|---|---|
| ⑭ | TV L |
| ⑮ | DAC out 2 |
| ⑯ | Rin |
| ⑰ | Cin |
| ⑱ | Lin |
| ⑲ | GND |
| ⑳ | CLOCK |
| ㉑ | DATA |
| ㉒ | W out |
| ㉓ | C out |
| ㉔ | L out |
| ㉕ | GND |
| ㉖ | R out |
| ㉗ | 9V |

**Fig. 3-5**

The Exclusive IC memory that memories adjustment values for $I^2C$ bus control sound multiplex IC is built in module, and this eliminates readjustment of the sound multiplex recontrol in the module-replacement.

## 1-6. CATV System AUTO MODE Decision

In the initial state (shipping and AC ON), the channel selection is carried out in the STD mode and the pull in operation is carried out by the sync and AFT signals. By this time, offset value from STD mode is memorized.

Two memories, memory 1 and memory 2, are required for the channels 5, 6 and the channels other than the channels 5, 6. A cable mode is decided by this offset values memorized and the start frequency of next channel selection is determined. The offset value is updated each time. The criterion of the decision and the start frequency are shown in tables 3-1 and 3-2.

**Table 3-1 Channels other than the channels 5, 6ch**

| Offset values | Decision | Start frequency |
|---|---|---|
| +0.75 ~ +2.5 MHz | NEW | fo +1.75 MHz |
| -0.75 ~ +0.75 MHz | STD/IRC | fo |
| -2.25 ~ -0.75 MHz | HRC | fo -1.25 MHz |

**Table 3-2 Channels 5, 6**

| Offset values | Decision | Start Frequency |
|---|---|---|
| +1.375 ~ +2.5 MHz | 5, 6ch IRC | fo +2.00 MHz |
| +0.5 ~ +1.375 MHz | 5, 6ch HRC | fo +0.75 MHz |
| -0.5 ~ +0.5 MHz | 5, 6ch STD | fo |
| -2.25 ~ -0.5 MHz | 5, 6ch OTHER | fo -1.00 MHz |

# 2. IF/RF CIRCUIT TROUBLESHOOTING

## 2-1. No Picture of VHF/UHF (Main Screen)

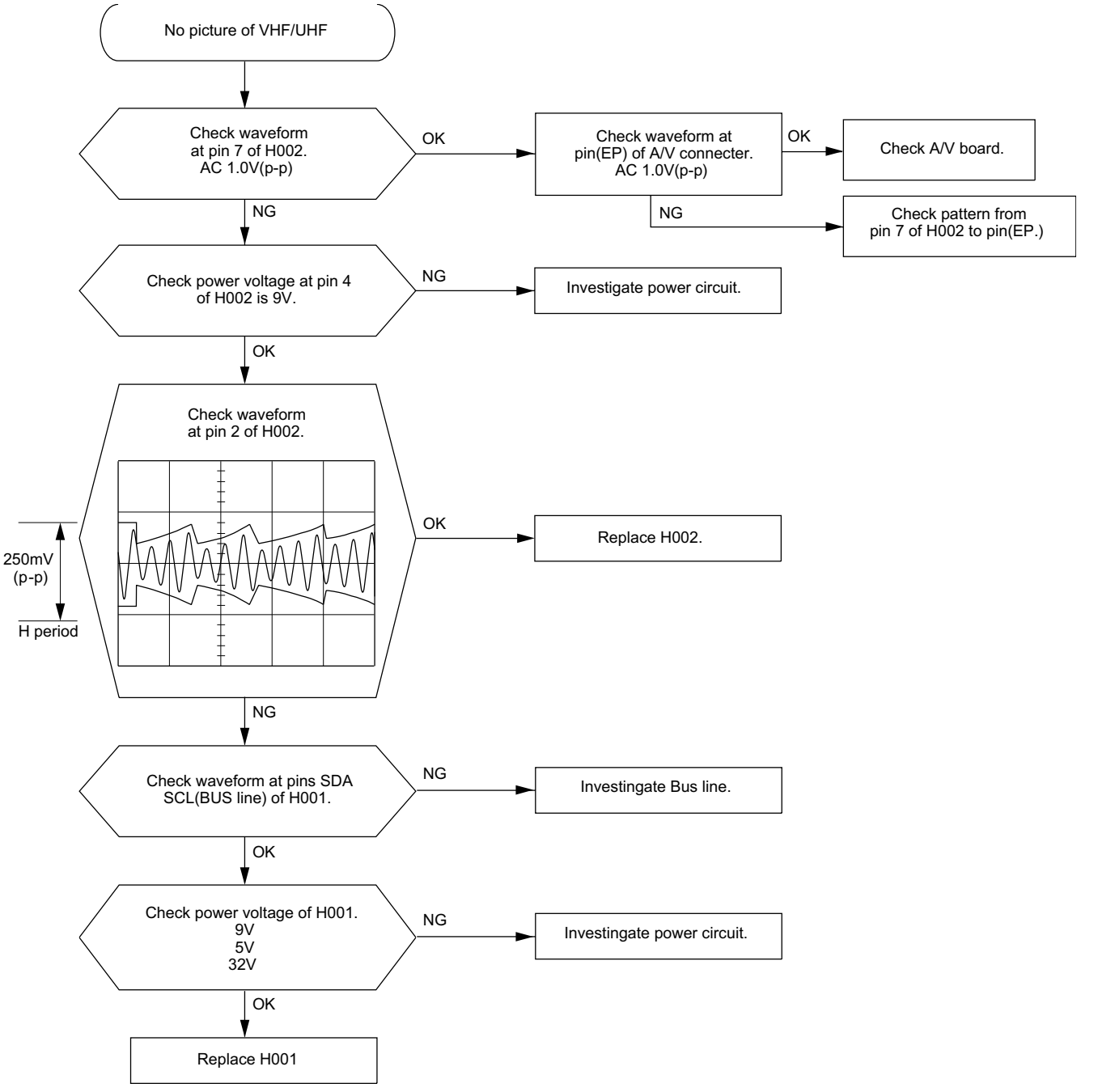



**Fig. 3-6**

## 2-2. No Picture of VHF/UHF (PIP Screen)

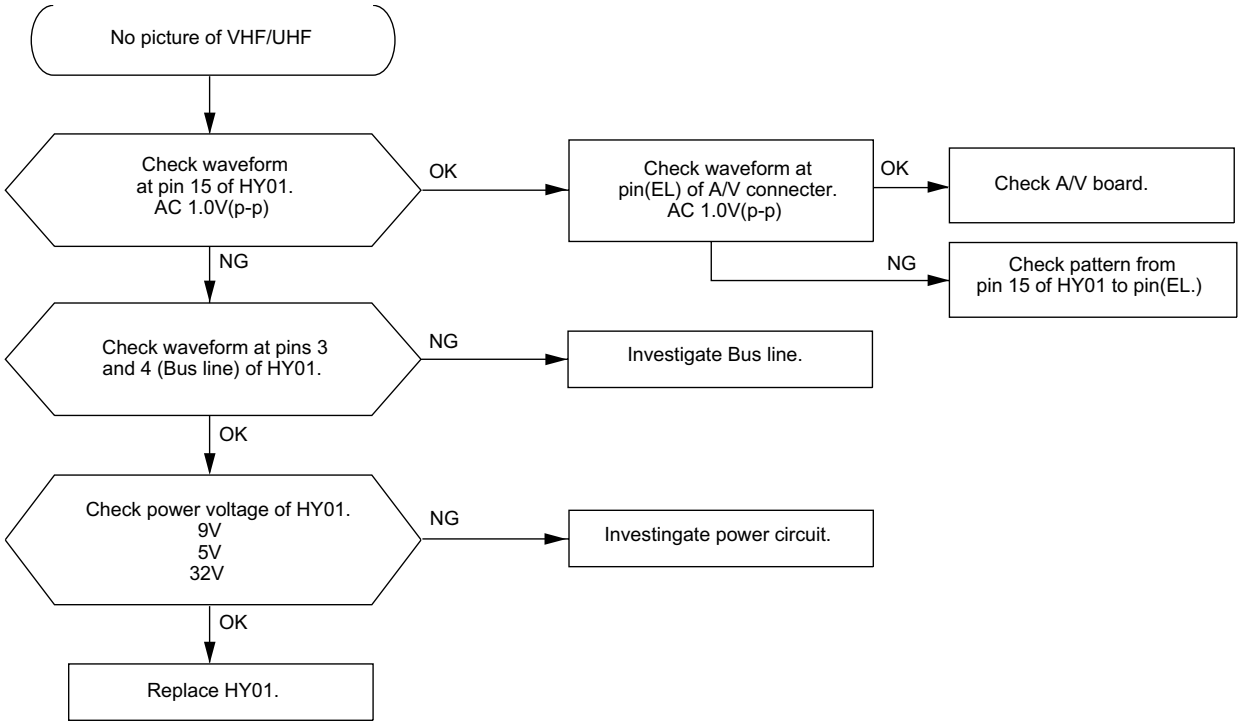



**Fig. 3-7**

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# SECTION IV
# CHANNEL SELECTION CIRCUIT

# 1. OUTLINE OF CHANNEL SELECTION CIRCUIT SYSTEM

The channel selection circuit in the N7SS chassis employs a bus system which performs a central control by connecting a channel selection microcomputer to a control IC in each circuit block through control lines called a bus. In the bus system which controls each IC, the $I^2C$ bus system (two line bus system) developed by Philips Co. Ltd. in the Netherlands has been employed.

The ICs controlled by the $I^2C$ bus system are : IC for audio signal processing (QN06), IC for V/C/D signal processing (Q501), IC for A/V switching (QV01), IC for non volatile memory (QA02), Main and sub U/V tuners (H001, HY01), IC for deflection distortion correction (Q302), IC for PIP signal processing (QY04), IC for closed caption control, A.PRO, I/O expander, JFORC, digital convergence, 3D YCS, SLC, V/C/D for PIP.

# 2. HARDWARE COMPONENT

**(1) Channel Selection Microprocessor**

The 8-bit single chip microprocessor (TLCS-870 series) is applied. The outline of the microprocessor is shown below.

- Production type name: TMPA8700CSN-113
- ROM: 60 k X 8 bits
- RAM: 2 k X 8 bits
- Package: SDIP42-P-600
- OTP built-in: TMPA8700PSN

**(2) Audio System Control IC (TOSHIBA TA1217AN)**

- Controls balance, sound quality adjustment such as high and low sounds and volume.
- Switches the SURROUND ON/OFF
- Switches SBS and perform level adjustment
- Switches audio mute

**(3) Video System Control IC (TOSHIBA TA1259N)**

- Controls video system such as CONTRAST, BRIGHTNESS, COLOR, TINT, SHARPNESS.
- Adjusts SUB COLOR, SUB BRIGHTNESS, SUB TINT and other video system parameter.
- Switches the modes for PICTURE PREFERENCE, COLOR TEMPERATURE.

**(4) External Input Switching SW IC (TOSHIBA TA8851CN)**

- Performs source switching for main and sub pictures.
- Switches total 4 systems of TV and video 3 inputs.

**(5) Memory IC (MICROCHIP 24LC08BI/P)**

- Memorizes the user last status for video and audio adjustment values, volume, external status, etc.
- Memorizes the parameters which determines the picture formation and distortion correction of the white balance data, deflection yoke data, etc.

**(6) U/V Tuner Control IC (MATSUSHITA EL466L)**

- Controls U/V channel selection frequency

**(7) 7DPC Unit Control IC (TOSHIBA TA1241N)**

- Performs pin-cushion distortion correction

**(8) PIP Control IC (TOSHIBA TC90A17F)**

- Performs sub picture ON/OFF, LOCATE, STILL, etc.

**(9) C/C Control Microprocessor (MITUBISHI M37274MX)**

- Performs CLOSED CAPTION mode switching

**(10) Digital Convergence Control IC**

- Performs digital convergence correction control
- Memorizes convergence data

**(11) 3D YCS Control IC (TOSHIBA TC90A28F)**

- Performs 3D YCS ON/OFF switching (at PIP ON)
- Performs 3D YCS operation control

**(12) Video IC for PIP (TOSHIBA TA1270F)**

- Adjusts the video system parameter of SUB COLOR, SUB BRIGHTNESS, SUB TINT, etc. for PIP

**(13) JFORC (183E2550AF02)**

- Controls picture compression/extension in vertical direction
- Controls picture vertical position

**(14) SLC (TOSHIBA TC90A04AF)**

- Converts in order

# 3. MICROCOMPUTER

Microcomputer TMPA8700CSN-113 has 60k byte of ROM capacity and equipped with OSD function inside.

The specification is as follow.

- Type name : TMPA8700CSN-113
- ROM : 60k byte
- RAM : 2k byte
- Processing speed : 0.5ms (at 8 MHz with shortest command)
- Package : 42 pin shrink DIP
- $I^2C$-BUS : two channels
- PWM : 14 bits X 1, 7 bits X 9
- ADC : 8 bits X 6 (Successive comparison system, Conversion time 20ms)

This microcomputer performs functions of AD converter, reception of U/V TV.

$I^2C$ device controls through $I^2C$ bus. (Timing chart : See Fig. 4-1)

- LED uses big current port for output only.
- For clock oscillation, 8 MHz ceramic oscillator is used.
- $I^2C$ has two channels. One is for $E^2$PROM only.
- Self diagnosis function which utilizes ACK function of $I^2C$ is equipped
- Function indication is added to service mode.
- Remote control operation is equipped, and the control by set no touch is possible. (Bus connector in the conventional bus chassis is deleted.)
- Substantial self diagnosis function

(1) B/W composite video signal generating function (micom inside)

(2) Generating function of audio signal equivalent to 1 kHz (micom inside)

(3) Detecting function of power protection circuit operation

(4) Detecting function of abnormality in IIC bus line

(5) Functions of LED blink indication and OSD indication

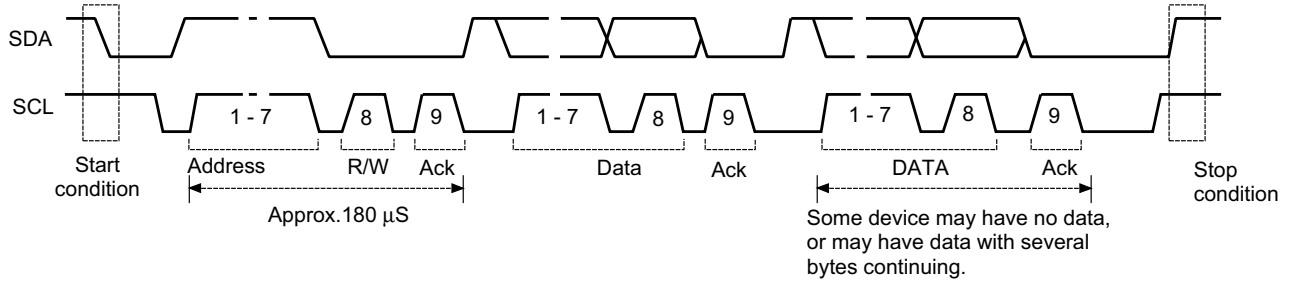



**Fig. 4-1**

## 3-1. Microcomputer Terminal Function

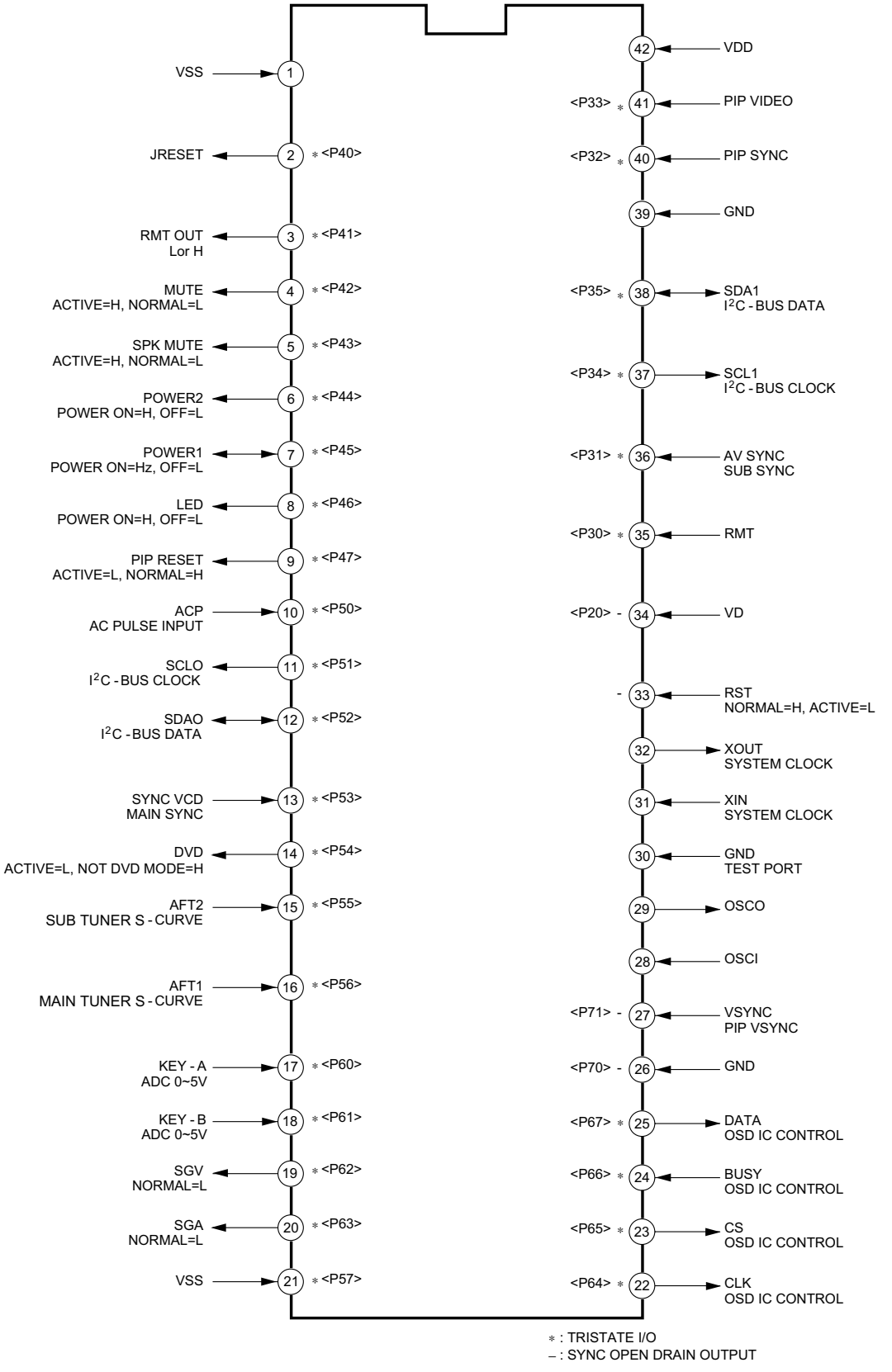



**Fig. 4-2**

## 3-2. Microcomputer Terminal Name and Operation Logic

**Table 4-1**

| Pin No. | Terminal Name | I/O | | | Functions & Logic |
|---|---|---|---|---|---|
| 1 | VSS | O | P4CR (OCH) | | Microcomputer GND, 0V connection |
| 2 | JRESET | O | P4CR (OCH) | D0=1 | Active = H, Normal = L |
| 3 | REM OUT | O | P4CR (OCH) | D1=1 | RMT output |
| 4 | MUTE | O | P4CR (OCH) | D2=1 | Sound mute output, Mute = H, Normal = L |
| 5 | SPK MUTE | O | P4CR (OCH) | D3=1 | Speaker mute, Mute = H, Noraml = L |
| 6 | POWER2 | O | P4CR (OCH) | D4=1 | DEF power control, POW ON = H, POW OFF = L |
| 7 | POWER1 | I/O | P4CR (OCH) | D5=0/1 | Power supply control, POW ON: Hz, POW OFF: L |
| 8 | LED | O | P4CR (OCH) | D6=1 | LED control, ON: H, Reset: L |
| 9 | PIP RST | O | P4CR (OCH) | D7=1 | PIP reset, ON: H, OFF: L |
| 10 | ACP | I | P5CR1 (09H) | D0=1 | AC pulse input |
| 11 | SCL0 | O | P5CR2 (FAEH) | D1=0 | Non volatile memory $I^2C$-bus clock, rising sync |
| 12 | SDA0 | I | P5CR2 (FAEH) | D2=0 | Non volatile memory $I^2C$ bus data |
| 13 | SYNC VCD | I | P5CR1 (09H) | D3=0 | Main sync, negative logic |
| 14 | DVD | O | P5CR1 (09H) | D4=0 | DVD mode switching, L: at color difference input, H: normal |
| 15 | AFT2 | I | P5CR1 (09H) | D5=0 | Sub tuner AFT, S character input |
| 16 | AFT1 | I | P5CR1 (09H) | D6=0 | Main tuner AFT, S character input |
| 17 | KEY-A | O | P6CR (0DH) | D0=0/1 | Local key A control, 0 ~5V |
| 18 | KEY-B | O | P6CR (0DH) | D1=0/1 | Local key B control, 0 ~ 5V |
| 19 | SGV | O | P6CR (0DH) | D2=1 | Test pattern output, Noraml: L |
| 20 | SGA | O | P6CR (0DH) | D3=1 | Test audio output, Normal:L Active:1 kHz squarewave |
| 21 | OSD RESET | O | P5CR1 (09H) | D7=1 | OSD IC reset, Normal: H, Reset: L |
| 22 | OSD CLK | O | P6CR (0DH) | D4=1 | OSD IC control clock, CLK frequency: approx. 20 kHz |
| 23 | OSD CS | O | P6CR (0DH) | D5=1 | ODS IC control CS, Active: L |
| 24 | OSD BUSY | I | P6CR (0DH) | D6=0 | OSD IC busy, Normal: L, Busy: H |
| 25 | OSD DATA | O | P6CR (0DH) | D7=1 | OSD IC control data |
| 26 | VSS | I | P7 (07H) | D0=1 | 0V |
| 27 | VSYNC | I | P7 (07H) | D1=1 | PIP vertical sync pulse detection for V-CHIP |
| 28 | OSCI | I | | D2=1 | Not used. |
| 29 | OSCO | O | | D3=0 | Not used. |
| 30 | GND | I | — | — | Micorcomputer shipping test |
| 31 | XIN | I | — | — | System clock |
| 32 | XOUT | O | — | — | oscillation connection terminal (8 Hz) |
| 33 | RST | I | — | — | Hard reset terminal, negative logic |
| 34 | VD | I | P2 (02H) | D0=1 | Vertical sync pulse detection |
| 35 | RMT | I | P3 (03H) | D0=0 | Remote control signal detection , Negative logic |
| 36 | AV SYNC | I | P3 (03H) | D1=1 | RF sync judgement, Sync: H, No sync: L |
| 37 | SCL1 | O | P3 (03H) | D4=1 | I2C bus clock, rising sync |
| 38 | SDA1 | I/O | P3 (03H) | D5=1 | I2C bus data |
| 39 | GND | I | — | — | Slicer ground, 0V connection |
| 40 | PIP SYNC | I | — | — | V-CHIP |
| 41 | PIP VIDEO | I | — | — | terminal |
| 42 | VDD | I | — | — | Microcomputer power supply 5V |

# 4. E²PROM (QA02)

E²PROM (non-volatile memory) has function which, in spite of power-off, memorizes the such condition as channel selecting data, last memory status, user control and digital processor data. The capacity of E²PROM is 8k bits.

Type name is 24LC08BI/P or ST24C08CB6, and those are the same in pin allocation and function, and are exchangeable each other. This IC controls through I²C bus. The power supply of E²PROM and MICOM is common. Pin function of E²PROM is shown in Fig. 4-3.

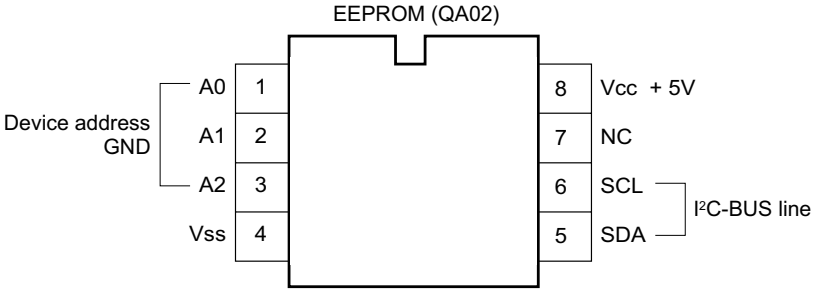



**Fig. 4-3**

# 5. ON SCREEN FUNCTION

ON SCREEN FUNCTION indicates data like channel, volume. RGBI and I/M signals are output from QR60 by the control from QA01. These signals are input to Q501 and displayed on a screen.

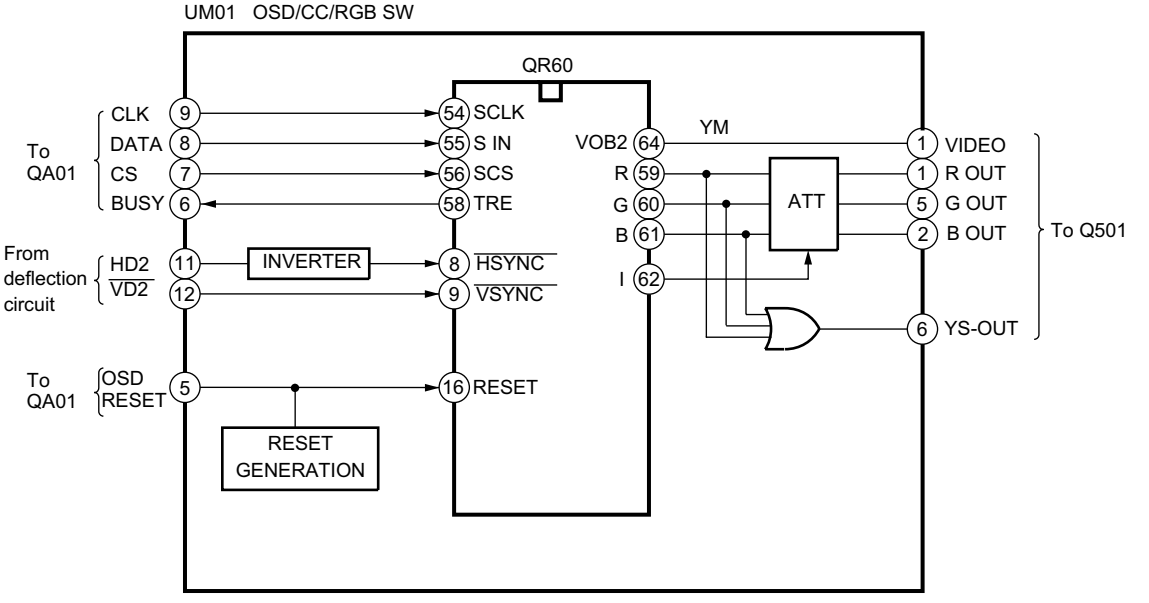



**Fig. 4-4**

# 6. SYSTEM BLOCK DIAGRAM

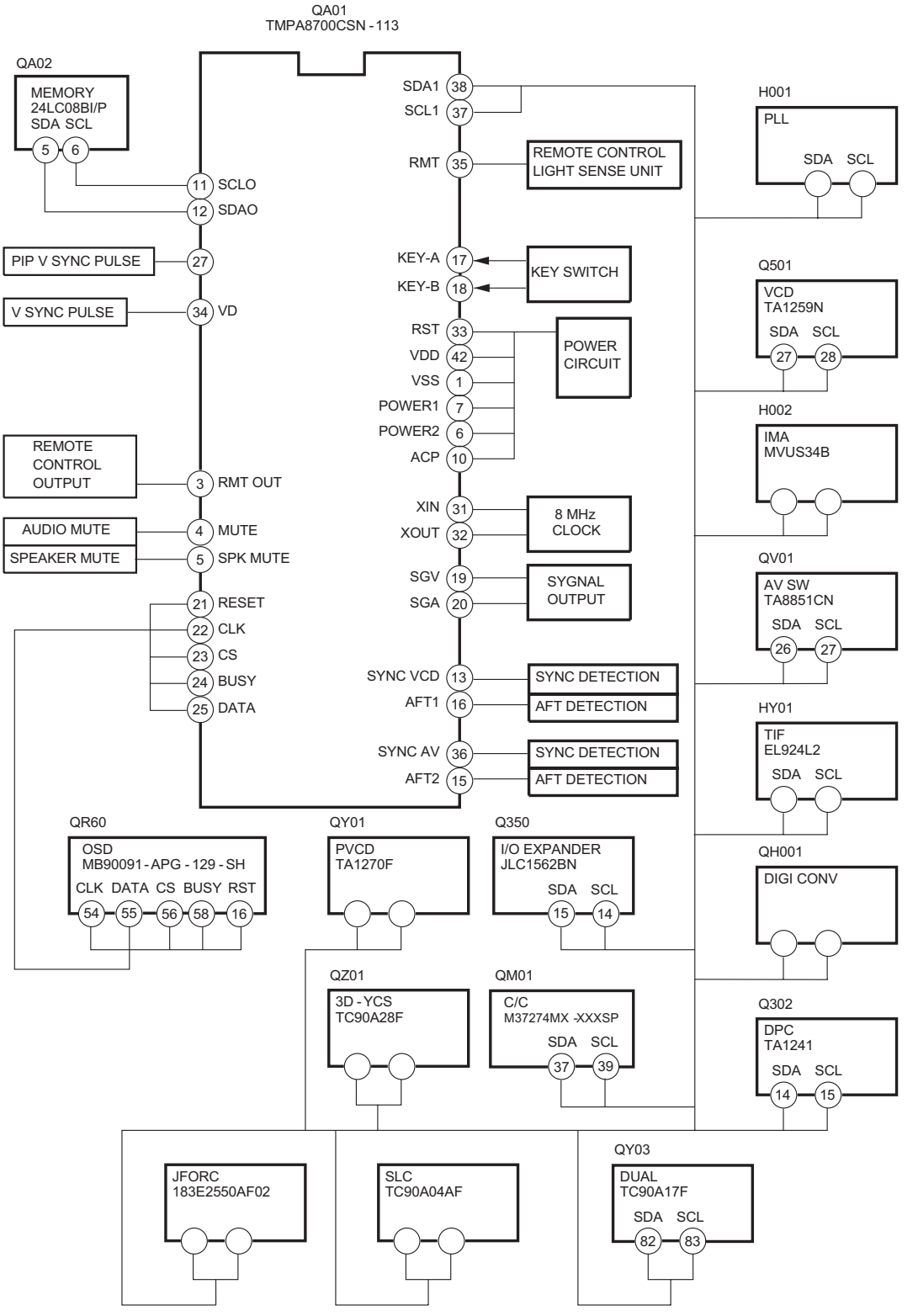



**Fig. 4-5**

# 7. LOCAL KEY DETECTION METHOD

Local key detection in the N7SS chassis is carried out by using analog like method which detects a voltage appears at local key input terminals (pins 17, 18) of the microcomputer when a key is pushed. With this method using two local key input terminals (pins 17, 18), key detection up to maximum 14 keys will be carried out.

The circuit diagram shown left is the local key circuit. As can be seen from the diagram, when one of key among SA-01 to SA-08 is pressed, each of two input terminal (pins 17, 18) developes a voltage $V_{IN}$ corresponding to the key pressed. (The voltage measurement and key identification are carried out by an A/D converter inside the microcomputer and the software.

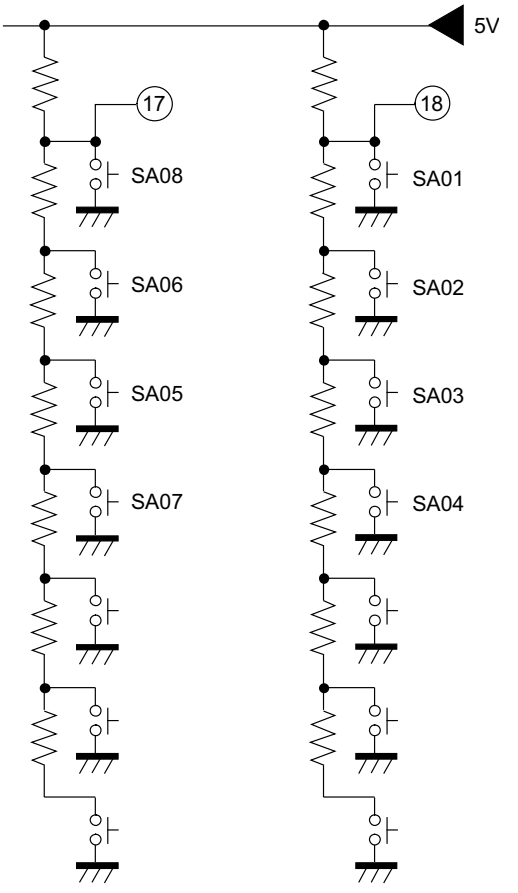



**Fig. 4-6 Local key assignment**

**Table 4-2 Local key assignment**

| Key No. | Function | Key No. | Function |
|---|---|---|---|
| SA01 | DEMO START/STOP | SA-05 | VOL UP |
| SA-02 | POWER | SA-06 | VOL DN |
| SA-03 | CH UP | SA-07 | ANT/VIDEO, ADV |
| SA-04 | CH DN | SA-08 | MENU |

# 8. REMOTE CONTROL CODE ASSIGNMENT

**Table 4-3**

| Code | CUSTOM CODES ARE 40-BFH<br>Function | Applicable to remote control | Applicable to TV set | Conti-nuty |
|---|---|---|---|---|
| 00H | 0 Channel | ○ | ○ | |
| 01H | 1 Channel | ○ | ○ | |
| 02H | 2 Channel | ○ | ○ | |
| 03H | 3 Channel | ○ | ○ | |
| 04H | 4 Channel | ○ | ○ | |
| 05H | 5 Channel | ○ | ○ | |
| 06H | 6 Channel | ○ | ○ | |
| 07H | 6 Channel | ○ | ○ | |
| 08H | 8 Channel | ○ | ○ | |
| 09H | 8 Channel | ○ | ○ | |
| 0AH | 100 Channel | ○ | ○ | |
| 0BH | ANT 1/2 | | ○ | |
| 0CH | RESET | ○ | ○ | |
| 0DH | AUDIO | | ○ | |
| 0EH | PICTURE/FUNC | | ○ | |
| 0FH | TV/VIDEO | ○ | ○ | |
| 10H | MUTE | ○ | ○ | |
| 11H | CHANNEL SEARCH | | ○ | |
| 12H | POWER | ○ | ○ | |
| 13H | MTS | | ○ | |
| 14H | ADD/ERASE | | | |
| 15H | TIMER/CLOCK | ○ | ○ | |
| 16H | AUTO PROGRAM | | | |
| 17H | CHANNEL RETURN | ○ | ○ | |
| 18H | DSP/SUR (TV/CATV) | | ○ | |
| 19H | CONTROL UP | ○ | ○ | ○ |
| 1AH | VOLUME UP | ○ | ○ | ○ |
| 1BH | CHANNEL UP | ○ | ○ | ○ |
| 1CH | RECALL | ○ | ○ | |
| 1DH | CONTROL DOWN | ○ | ○ | ○ |
| 1EH | VOLUME DOWN | ○ | ○ | ○ |
| 1FH | CHANNEL DOWN | ○ | ○ | ○ |
| 40H | PIP LOCATE ↑ | | | |
| 41H | PIP LOCATE ↓ | | | |
| 42H | PIP LOCATE → | | | |
| 43H | PIP LOCATE ← | | | |
| 44H | CARVER | | | |
| 45H | SURROUND UP | | | |
| 46H | SURROUND DOWN | | | |
| 47H | VOCAL ZOOM | | | |
| 48H | CHANNEL LOCK | | | |
| 49H | | | | |
| 4AH | PIP CHANNEL UP | | ○ | ○ |
| 4BH | PIP CHANNEL DOWN | | ○ | ○ |
| 4CH | PIP STILL/RELEASE | ○ | ○ | |
| 4DH | PIP ZOOM, ZOOM SIZE | | | |
| 4EH | PIP LOCATE (CH SEARCH) | | ○ | ○ |
| 4FH | PIP SOURCE | ○ | ○ | |

| Code | Custom codes are 40-BFH<br>Function | Applicable to remote control | Applicable to TV set | Conti-nuty |
|---|---|---|---|---|
| 50H | PIP STILL | ○ | ○ | |
| 51H | PIP ON/OFF | ○ | ○ | |
| 52H | Do not use. Old type core power ON | | | |
| 53H | PIP SWAP | ○ | ○ | |
| 54H | PIC SIZE | | | |
| 55H | DSP F/R | ○ | ○ | |
| 56H | WIDE/SCROLL | | | |
| 57H | CAPTION | ○ | ○ | |
| 58H | EXIT | ○ | ○ | |
| 59H | CYCLONE, SBS | | ○ | |
| 5AH | SET UP | | ○ | |
| 5BH | OPTION | | | |
| 5CH | SUB WOOFER UP | | | |
| 5DH | SUB WOOFER DOWN | | | |
| 5EH | | | | |
| 5FH | | | | |
| 80H | MENU | ○ | ○ | |
| 81H | EDS | | | |
| 82H | ADV UP | ○ | ○ | |
| 83H | ADV DWN | ○ | ○ | |
| 84H | | | | |
| 85H | GUIDE | | | |
| 86H | THEME | | | |
| 87H | LIST | | | |
| 88H | PIP CONTROL | | | |
| 89H | ENTER/TUNE | ○ | ○ | |
| 8AH | PAGE UP | | | |
| 8BH | DATA UP | | | |
| 8CH | PAGE DN | | | |
| 8DH | DATA DN | | | |
| 8EH | CANCEL | | | |
| 8FH | REC | | | |
| 90H | | | | |
| 91H | | | | |
| 92H | Do not use. Old type core on. | | | |
| 93H | | | | |
| 94H | | | | |
| 95H | | | | |
| 96H | | | | |
| 97H | NOISE CLEAN | | | |
| 98H | | | | |
| 99H | | | | |
| 9AH | PIP VOLUME UP | | | |
| 9BH | | | | |
| 9CH | PIP CONTROL | | | |
| 9DH | | | | |
| 9EH | PIP VOLUME DOWN | | | |
| 9FH | | | | |

| Code | Custom codes are 40-BFH | | |
|---|---|---|---|
| | Function | Applicable to TV set | Conti-nuty |
| A0H | SUB-BRIGHT ADJUSTMENT | ○ | |
| A1H | G. DRIVE ADJUSTMENT | ○ | |
| A2H | B. DRIVE ADJUSTMENT | ○ | |
| A3H | | | |
| A4H | CUTOFF DRIVE 40H INITIALIZING, SCREEN, ADJ. | ○ | |
| A5H | R. CUTOFF ADJUSTMENT | ○ | |
| A6H | G. CUTOFF ADJUSTMENT | ○ | |
| A7H | B. CUTOFF ADJUSTMENT | ○ | |
| A8H | MEMORY ALL AREA INITIALIZE | ○ | |
| A9H | PIP BRIGHT ADJUSTMENT | ○ | |
| AAH | SUB CONTRAST ADJUSTMENT | ○ | |
| ABH | HOR, VER PICTURE POSITON ADJUSTMENT | ○ | |
| ACH | SUB COLOR ADJUSTMENT | ○ | |
| ADH | SUB TINT ADJUSTMNET | ○ | |
| AEH | ADJUSTMENT-UP | ○ | ○ |
| AFH | ADJUSTMENT-DOWN | ○ | ○ |
| B0H | SCREEN ADJ.: SERVICE | ○ | |
| B1H | DSP ON/OFF | ○ | |
| B2H | TEXT-1 | ○ | |
| B3H | TV/PIP VIDEO CHANGE-OVER | ○ | |
| B4H | CAPTION-1 | ○ | |
| B5H | | | |
| B6H | | | |
| B7H | TV/CABLE CHANGE-OVER IN SAME TIME ON MAN AND SUB | ○ | |
| B8H | HOTEL SETTING MENU | | |
| B9H | DATA 4 TIMES SPEED UP | ○ | ○ |
| BAH | DATA 4 TIMES SPEED DOWN | ○ | ○ |
| BBH | CHANGE-OVER OF HOTEL/NORMAL | | |
| BCH | PIP CENTER | ○ | |
| BDH | M MODE | ○ | |
| BEH | CAPTON OFF | ○ | |
| BFH | ALL CHANNEL PRESET | ○ | |
| C0H | | | |
| C1H | DIRECT WIDE 1 | | |
| C2H | DIRECT FULL | | |
| C3H | | | |
| C4H | | | |
| C5H | | | |
| C6H | | | |
| C7H | | | |
| C8H | | | |
| C9H | | | |
| CAH | | | |
| CBH | | | |
| CCH | | | |
| CDH | | | |
| CEH | | | |
| DFH | | | |

| Code | Custom codes are 40-BFH | | |
|---|---|---|---|
| | Function | Applicable to TV set | Conti-nuty |
| D0H | | | |
| D1H | | | |
| D2H | Do not use. Old type core power ON | | |
| D3H | | | |
| D4H | | | |
| D5H | | | |
| D6H | | | |
| D7H | PIP VIDEO ADJ. | | |
| D8H | STILL, FRAME ADVANCE | | |
| D9H | | | |
| DAH | SPEED | | |
| DBH | | | |
| DCH | ZOOM | | |
| DDH | | | |
| DEH | | | |
| DFH | | | |
| E0H | PINCUTION/EW CORER (PARA/CNR) | ○ | |
| E1H | VERTICAL S-CUVE CORRECTIONVERTICAL M-CURVE CORRECTION (VSC/FVC) | ○ | |
| E2H | | | |
| E3H | | | |
| E4H | | | |
| E5H | | | |
| E6H | | | |
| E7H | | | |
| E8H | | | |
| E9H | | | |
| EAH | HORIZONTAL WIDTH (WID/PARA) | ○ | |
| EBH | TRAPEZOIDE CORRECTION (TRAP) | ○ | |
| ECH | TEST TONE | | |
| EDH | DOLBY | | |
| EEH | 3 DIMENTIONAL Y/C SEPARATION | | |
| EFH | DPC | | ○ |
| E0H | STANDARD (HEIGHT LINEARITY) (VLIN/HIT) | ○ | |
| E1H | WIDE (HEIGHT LINEARITY) (VLIN) | ○ | |
| F2H | SCROOL | | |
| F3H | WIDE 1, 2, 3 | | |
| F4H | | | |
| F5H | | | |
| F6H | | | |
| F7H | | | |
| F8H | | | |
| F9H | | | |
| FAH | | | |
| FBH | | | |
| FCH | | | |
| FDH | | | |
| FEH | | | |
| FFH | | | |

## 9. ENTERING TO SERVICE MODE

(1) Procedures

1) Press once MUTE key of remote hand unit to indicate MUTE on screen.
2) Press again MUTE key of remote hand unit to keep pressing until the next procedure.
3) In the status of above (2), wait for disappearing of indication on screen.
4) In the status of above (3), press MENU (Channel setting) key on TV set.

(2) Service mode is not memorized as the last-memory.

(3) During service mode, indication S is displayed at upper right corner on screen.

## 10. TEST SIGNAL SELECTION

(1) In OFF state of test signal, SGA terminal (Pin 20) and SGV terminal (Pin 21) are kept "L" condition.

(2) The function of VIDEO test signal selection is cyclically changed with VIDEO key (remote unit).

**Table 4-4**

| Test signal No. | Name of pattern |
|---|---|
| 0 | Signal OFF |
| 1 | All black signal + R single color (OSD) |
| 2 | All black signal + G single color (OSD) |
| 3 | All black signal + B single color (OSD) |
| 4 | All black signal |
| 5 | All white signal |
| 6 | W/B |
| 7 | Black cross bar |
| 8 | White cross bar |
| 9 | Black cross hatch |
| 10 | White cross hatch |
| 11 | Black cross dot |
| 12 | White cross dot |

(3) SGA (audio test signal) output should be square wave of 1 kHz.

## 11. SERVICE ADJUSTMENT

(1) ADJUSTMENT MENU INDICATION ON/OFF : MENU key (on TV set)

(2) During display of adjustment menu, the followings are effective.

1) Selection of adjustment item :
POS UP/DN key (on TV/Remote unit)
2) Adjustment of each item :
VOL UP/DN key (on TV/ Remote unit)
3) Direct selection of adjustment item
R CUTOFF: 1 POS (Remote unit)
G CUTOFF: 2 POS (Remote unit)
B CUTOFF: 3 POS (Remote unit)
4) Data setting for PC unit adjustment
SUB CONTRAST: 4 POS (Remote unit)
SUB COLOR: 5 POS (Remote unit)
SUB TINT: 6 POS (Remote unit)
5) Screen adjustment mode ON/OFF: VIDEO (TV)
6) Test signal selection: VIDEO (Remote unit)

* In service mode, serviceable items are limited.

(3) Test audio signal ON/OFF: 8 POS (Remote unit)
* Test audio signal: 1 kHz

(4) Self check display: 9 POS (Remote unit)
* Cyclic display (including ON/OFF)

(5) Initialization of memory :
CALL (Remote unit) + POS UP (TV)

(6) Initialization of self check data :
CALL (Remote unit) + POS DN (TV)

(7) BUS OFF :
CALL (Remote unit) + VOL UP (TV)

(8) Convergence adjustment pattern: 7 POS
Pushing once: Convergence adjustment mode
Pushing twice: Data memory
Pushing three times: Escaping from pattern.

# 12. FAILURE DIAGNOSIS PROCEDURE

Model of N7SS chassis is equipped with self diagnosis function inside for trouble shooting.

## 12-1. Contens to be Confirmed by Customer

**Table 4-5**

| Contents of self diagnosis | Display items and actual operation |
|---|---|
| A. DISPLAY OF FAILURE INFORMATION<br>IN NO PICTURE (Condition of display) | Power indicator lamp blinks and picture does not come. |
| 1. When power protection circuit operates; | 1. Power indicator red lamp blinks. (0.5 seconds interval) |
| 2. When I²C-BUS line is shorted; | 2. Power indicator red lamp blinks. (1 seconds interval)<br>If these indications appear, repairing work is required. |

## 12-2. Contents to be Confirmed in Service Work (Check in Self Diagnosis Mode)

**Table 4-6**

| Contents of self diagnosis | Display items and actual operation |
|---|---|
| Contents of self diagnosis<br><Countermeasure in case that phenomenon always arises.><br>B. Detection of shortage in BUS line<br>C. Check of communication status in BUS line<br>D. Check of signal line by sync signal detection<br>E. Indication of part code of microcom. (QA01)<br>F. Number of operation of power protection circuit | Display items and actual operation<br>(Example of screen display)<br>**SELF CHECK**<br>NO. 239XXXX ← Part coce of QA01 ← E<br>POWER: 000000 ← Number of operation of power protection circuit ← F<br>BUS LINE: OK ← Short check of bus line ← B<br>BUS CONT: OK ← Communication check of busline ← C<br>BLOCK: QV01, QV01S ← D |

## 12-3. Executing Self Diagnosis Function

### 12-3-1. Procedures

(1) Set to service mode.

(2) Pressing “9” key on remote unit displays self diagnosis result on screen.

Every pressing changes mode as below.

SERVICE mode → SELF DIAGNOSIS mode

(3) To exit from service mode, turn power off.

## 12-4. Understanding Self Diagnosis Function Indication

In case that phenomenon always arises. See Fig. 4-7 .

(Example of screen display)

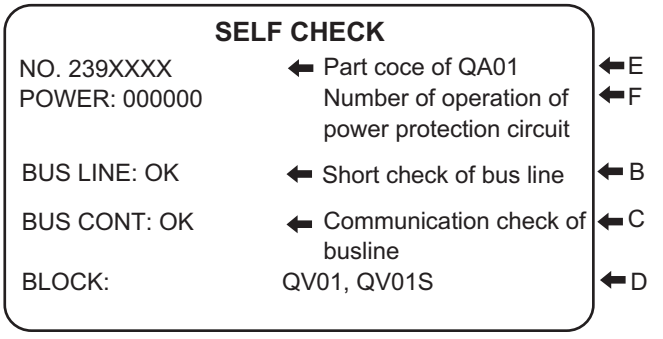



**Fig. 4-7**

**Table 4-5**

| Item | Contents | Instruction os results |
|---|---|---|
| BUS LIME | Detection of bus line short | Indication of OK for normal result, NG for abnormal |
| BUS CONT | Communication state of bus line | Indication of OK for normal result<br>Indication of failure place in abnormality<br>(Failure place to be indicated)<br>QA02 NG, H001 NG, Q501 NG, H002 NG<br>QV01 NG, Q302 NG, QY02 NG, HY01 NG<br>QD04 NG, QM01 NG, Q701 NG<br><br>QA02 $E^2$PROM, Q350 I/O EXP<br>H001 MTUN, QM30 C/C<br>Q501 VCD, QX40 JFORC<br>H002 MTS, Q701 DIG-CONV<br>QV01 AVSW, QZ01 YCS<br>Q302 E-WC, QX30 SLC<br>QY03 DUAL, QY01 PIP/VCD<br>HY01 PIP TUN, QK06 WAC<br><br>Note 1. The indication of failure place is only one place though failure places are plural. When repair of a failure place finishes, the next failure place is inndicated. (The order of priority of indication is left side.) |
| BLOCK: QV01<br>QV01S | The sync signal part in each video signal supplied from each block is detected. Then by checking the existence or non of sync part, the result of self diagnosis is displayed on screen. Besides, when "9" key on remote unit is pressed, diagnosis operation is first executed once. | *Indication by color<br>• Normal block : Green<br>• Non diagnosis block : Cyan |

### 13-4-1. Clearing Method of Self diagnosis Result

In the error count state of screen, press “CHANNEL DOWN” button on TV set pressing “Recall” button on remote unit.

**Caution:**

Allways keep the following caution, in the state of service mode screen.

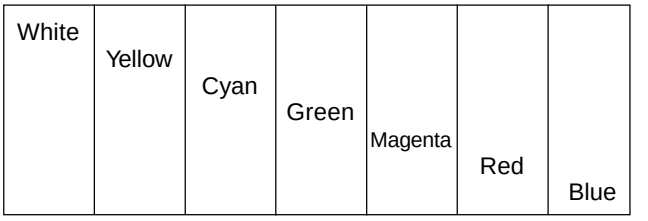
- Do not press “CHANNEL UP” button. This will cause initialization of memory IC. (Replacement of memory IC is required.
- Do not initialize self diagnosis result. This will change user adjusting contents to factory setting value. (Adjustment is required.)

### 13-4-2. Method Utilizing Inner Signal (VIDEO INPUT 1 terminal should be open.)

(1) With service mode screen, press VIDEO button on remote unit. If inner video signal can be received, QV01 and after are normal.

(2) With service mode screen, press “8” button on remote unit. If sound of 1 kHz can be heard, QV01 and after are normal.

* By utilizing signal of VIDEO input terminal, each circuit can be checked. (Composite video signal, audio signal)




( COLOR BAR SIGNAL)
Color elements are positioned in sequence of high brightness.

**Fig. 4-8**

# 13. TROUBLE SHOOTING CHART

## 13-1. TV does not turn ON.

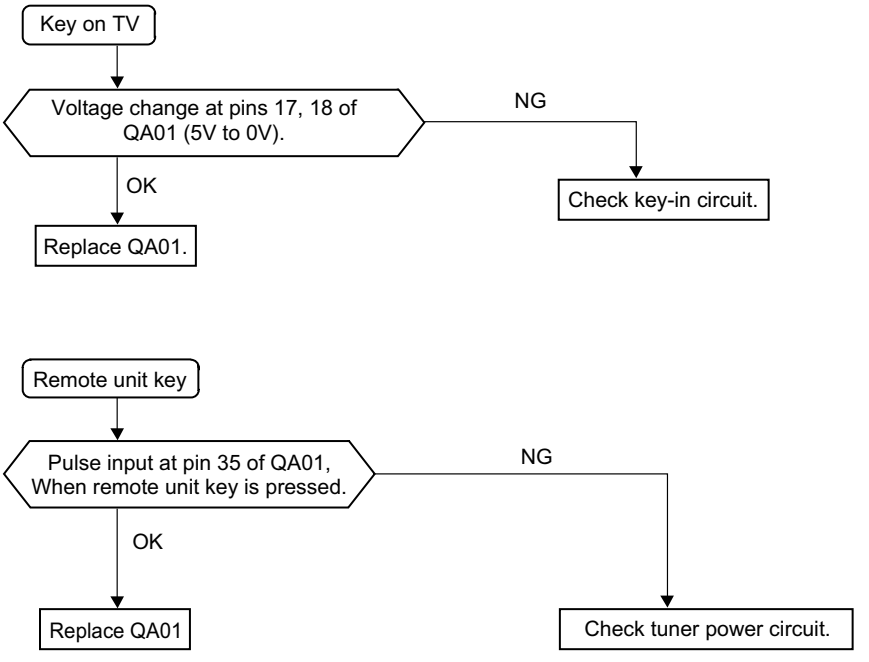



**Fig. 4-9**

## 13-2. No Acception of Key-IN

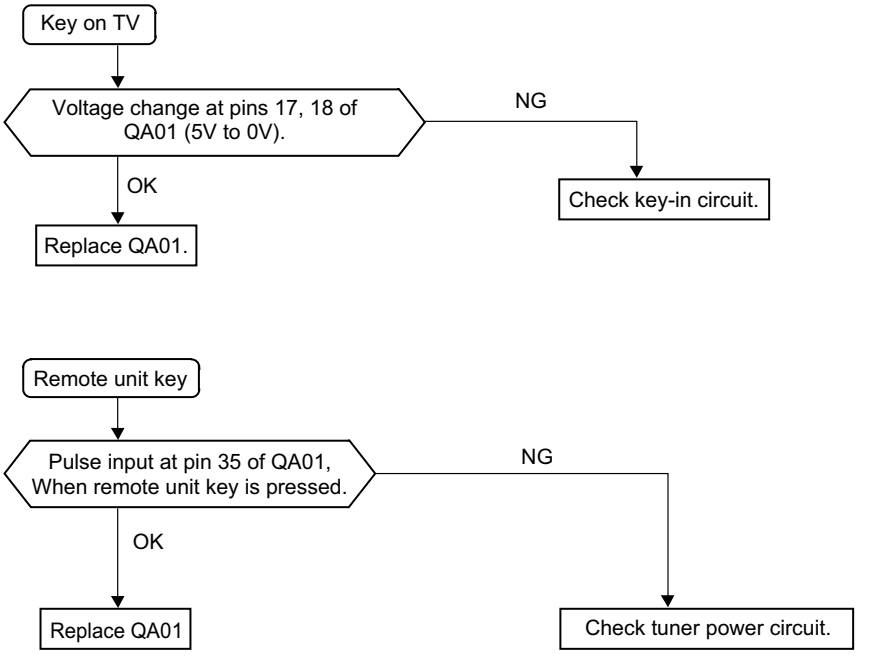



**Fig. 4-10**

## 13-3. No Picture (Snow Noise)

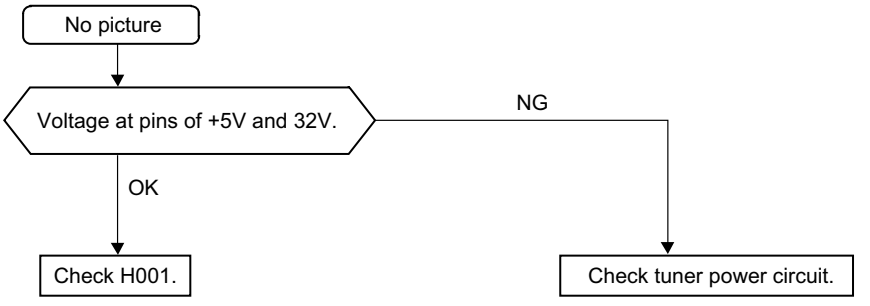



**Fig. 4-11**

## 13-4. Memory Circuit Check

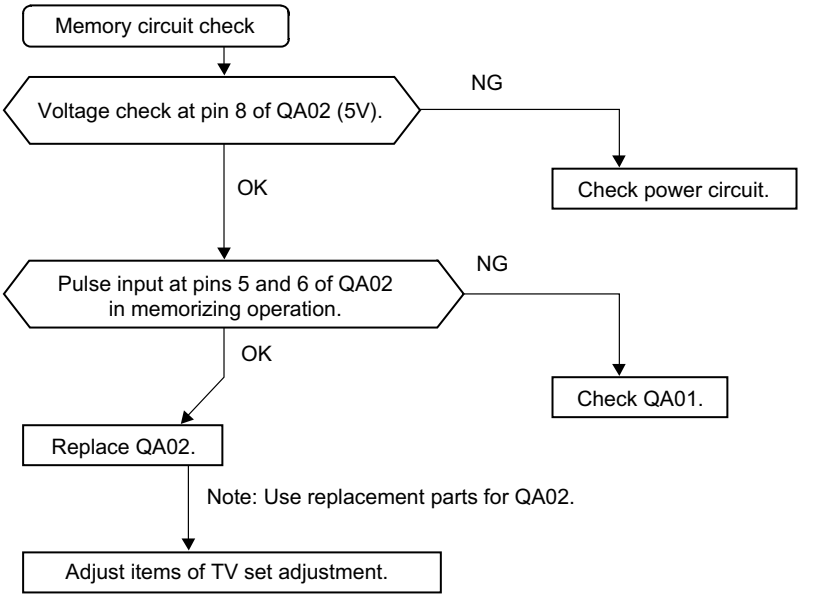



**Fig. 4-12**

## 13-5. No Indication on Screen

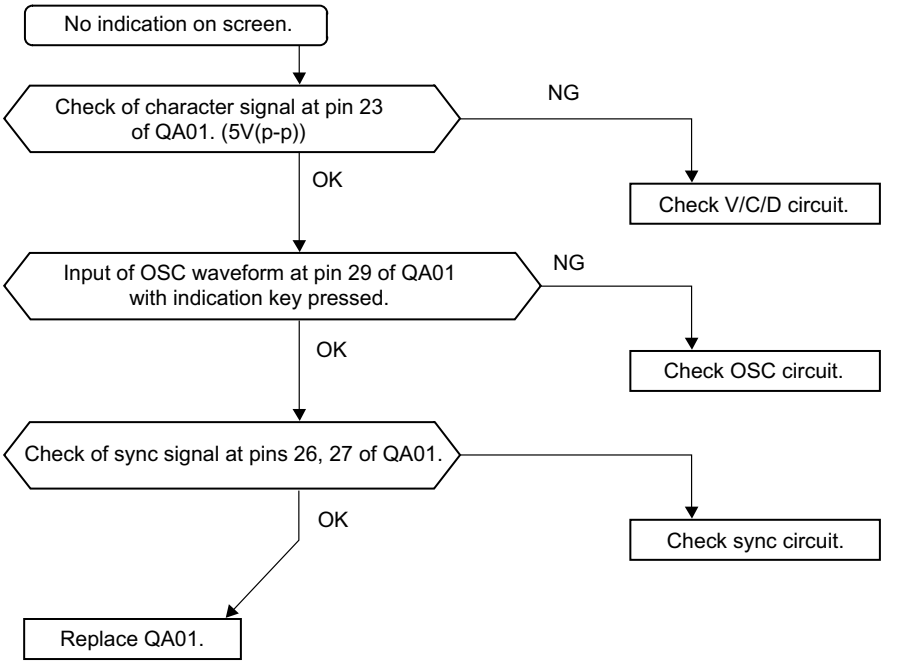



**Fig. 4-13**

# SECTION V
# VIDEO CIRCUIT

# 1. A/V SELECTOR CIRCUIT

## 1-1. General

The A/V selector circuit selects the video and audio signals from the tuner and external device. Selection of signals is controlled by the microcomputer through the $I^2C$ bus.

## 1-2. Speifications

**Table 5-1**

| | |
|---|---|
| Internal input | U/V tuner (Main)<br>U/V tuner (Sub) |
| External input | Video 1 (with S terminal)<br>Video 2<br>Video 3 (Front) (with S terminal) |
| Output | Video output (V, L, R) |

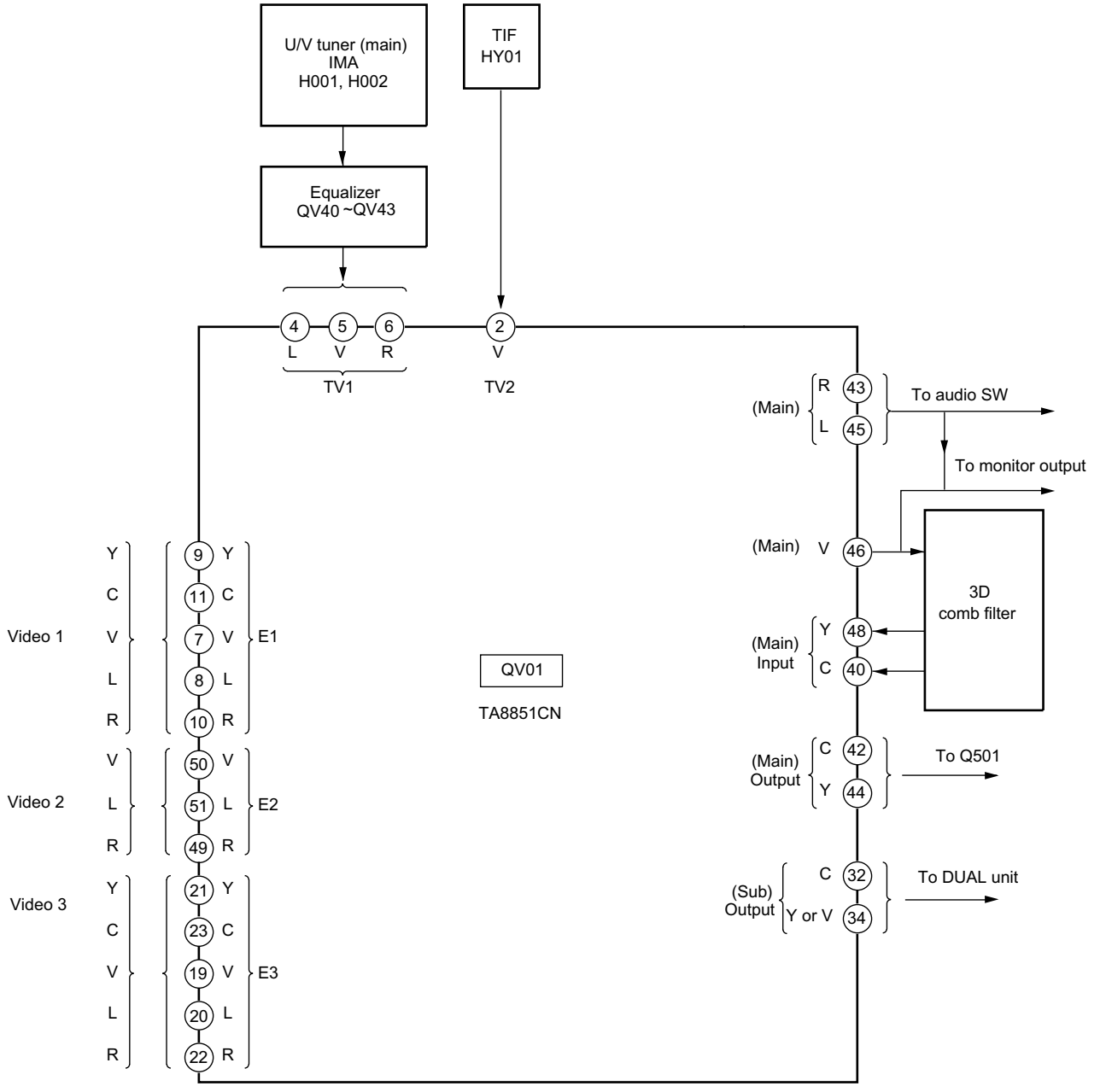



**Fig. 5-1 Block diagram of the A/V selector circuit**

## 1-3. Operation of the Circuit

### 1-3-1. Composite Video Signal

The selected video signal is sent to pin 46 of QV01, YC-separated through the comb filter, applied to pins 40 & 48 and output to pins 42 & 46 of QV01, then supplied to Q501 (V/C/D).

The video signal for the subscreen is sent to pins 32 and 34, then supplied to the dual unit.

### 1-3-2. S-video Signal

When the cable is connected to the S-terminal, the internal switch of the S-terminal is shorted with GND, each V-terminal (composite video terminal) of QV01 drops in bias level through the resistor, and QV01 sends the Y/C signal of the selected channel directly to pins 42 and 44.

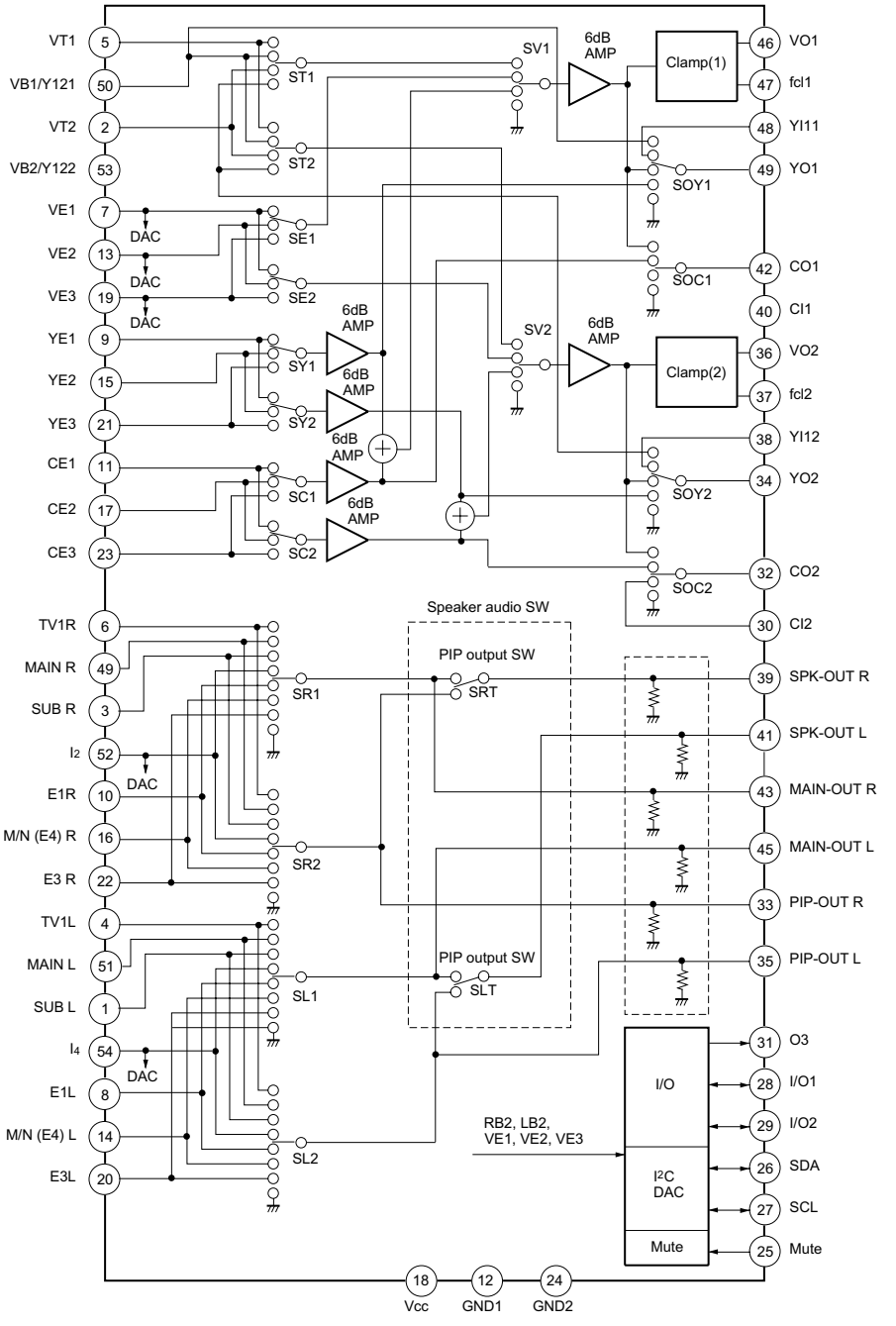



**Fig. 5-2 Block diagram of QV01 (TA8851CN)**

# 2. VIDEO PROCESSING CIRCUIT

## 2-1. General

Fig. 5-1 shows the video signal block diagram. The flow of signal is explained in this section. The video signal which is selected with the A/V selector circuit is applied to pins 15 and 13 of Q501 as Y/C signals. The Y-signal is unchanged, the C-signal is color demodulated with Q501, then the signals are sent to pins 4, 5 and 6 as a YIQ signal.

The YIQ signal is horizontally compressed in WAC, superimposed on the subscreen in DW, and applied to the UP CON, where it is double-speed converted and the horizontal frequency is converted to 31.5 kHz. The converted YIQ signal is sent to pins 53, 52 and 51 of Q501.

Q501 controls brightness, unicolor, color density and tone, corrects picture quality, and switches OSD and C/C, then the signal is developed from pins 43, 42 and 41 and applied to the CRT drive circuit.

## 2-2. V/C/D IC (Q501)

### 2-2-1. TA1259N

The video signal processing is carried out by Q501. The IC is improved to be a wide bandwidth mainly in the signal processing circuit so that the past IC (TA1222AN) may perform the video process for the up-converted NTSC signal. The following describes the main terminal information of Q501.

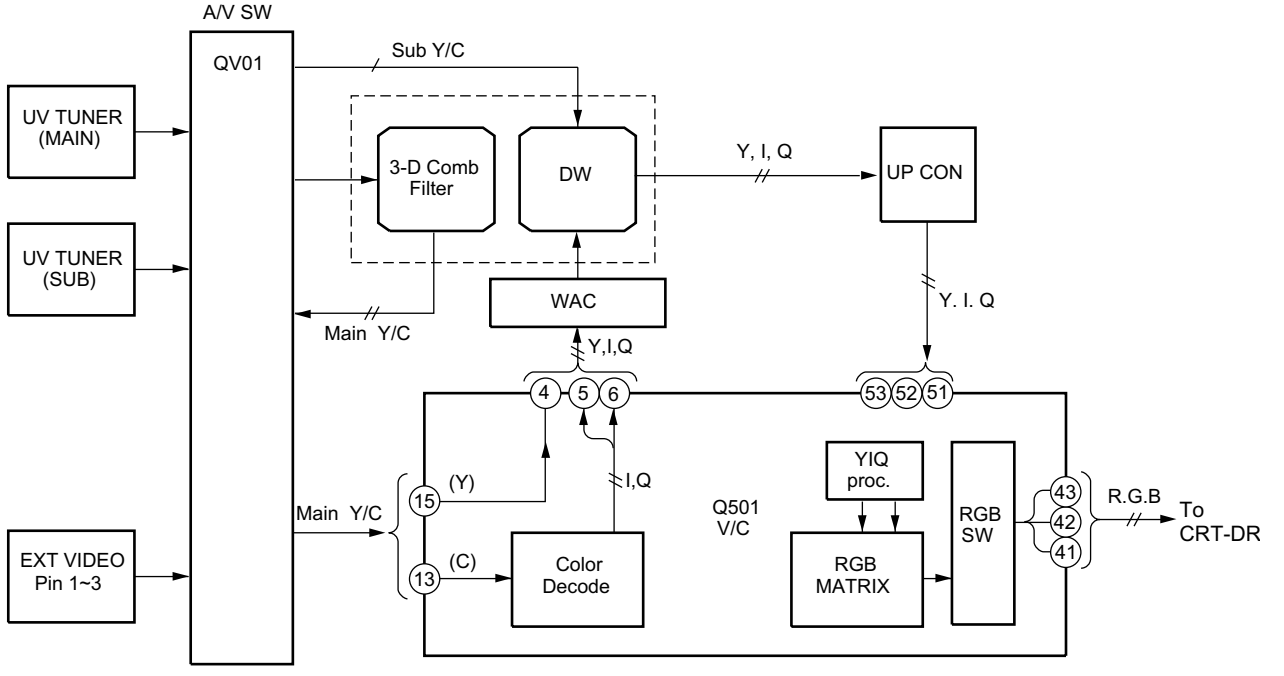



**Fig. 5-3**

**Table 5-2**

| Pin No. | Pin Name | Descriptions |
|---|---|---|
| 1 | CW output | 3.58 MHz signal synchronized with burst signal is output. |
| 2 | SCP output | The signal is superimposed by the burst gate pulse and the blanking pulse. The signal is used for the video signal clamping. |
| 10 | X'tal | 3.58 MHz oscillation crystal terminal. |
| 11 | APC filter | Phase detection terminal for color synchronization (also used for oscillation frequency control) |
| 17 | Sync input | Sync signal input terminal. Y signal is input. |
| 18 | Sync output | The sync signal sync-separated is output. Used for no signal detection in microcomputer. |
| 23 | Clamp input | Clamp pulse input terminal synchronized with Y signal input to pin 53. |
| 24 | Mask pulse input | Masking pulse input terminal for black extension prevention synchronized with Y signal input to pin 53. |
| 25 | Blanking input | Blanking pulse input terminal synchronised with Y signal input to pin 53. |
| 30 | HD output | Horizontal pulse synchronized with Y signal input to pin 15. |
| 31 | VD output | Vertical pulse synchronised with Y signal input to pin 15. |
| 32 | YS input | Switching pulse for multi-language broadcast display. |
| 36 | OSD-YS input | Switching pulse for OSD display. |
| 45 | ABL input | ABL control input terminal. |
| 47 | YM input | Half tone switching pulse at OSD display. |
| 49 | APL detection | Detects an average level of the video signal for direct current transmission correction. |
| 50 | Black detection | Black area of the video signal for black extension circuit is detected. |
| 54 | COL | Used for color limiter peak hold. |
| 55 | DAC 1 | Test point (TP501). In service mode, adjustment waveform is observed. |

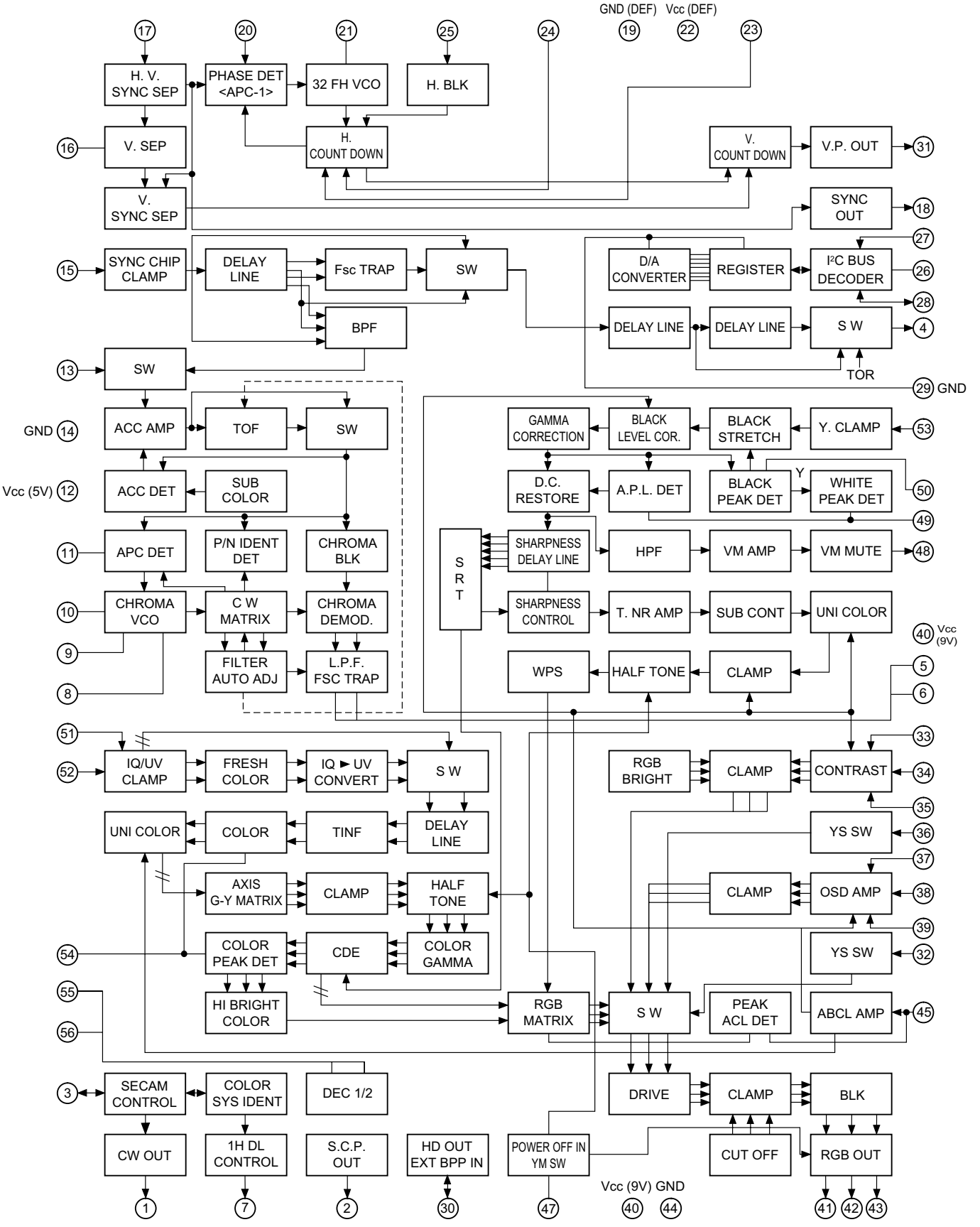

GND (DEF)
Vcc (DEF)
H. V. SYNC SEP
PHASE DET <APC-1>
32 FH VCO
H. BLK
V. SEP
H. COUNT DOWN
V. COUNT DOWN
V.P. OUT
V. SYNC SEP
SYNC OUT
SYNC CHIP CLAMP
DELAY LINE
Fsc TRAP
SW
BPF
D/A CONVERTER
REGISTER
I²C BUS DECODER
DELAY LINE
DELAY LINE
S W
TOR
GND
ACC AMP
TOF
SW
GAMMA CORRECTION
BLACK LEVEL COR.
BLACK STRETCH
Y. CLAMP
ACC DET
SUB COLOR
D.C. RESTORE
A.P.L. DET
BLACK PEAK DET
WHITE PEAK DET
APC DET
P/N IDENT DET
CHROMA BLK
S R T
SHARPNESS DELAY LINE
HPF
VM AMP
VM MUTE
CHROMA VCO
C W MATRIX
CHROMA DEMOD.
SHARPNESS CONTROL
T. NR AMP
SUB CONT
UNI COLOR
FILTER AUTO ADJ
L.P.F. FSC TRAP
WPS
HALF TONE
CLAMP
IQ/UV CLAMP
FRESH COLOR
IQ ► UV CONVERT
S W
RGB BRIGHT
CLAMP
CONTRAST
UNI COLOR
COLOR
TINF
DELAY LINE
YS SW
AXIS G-Y MATRIX
CLAMP
HALF TONE
CLAMP
OSD AMP
COLOR PEAK DET
CDE
COLOR GAMMA
YS SW
HI BRIGHT COLOR
RGB MATRIX
S W
PEAK ACL DET
ABCL AMP
SECAM CONTROL
COLOR SYS IDENT
DEC 1/2
DRIVE
CLAMP
BLK
CW OUT
1H DL CONTROL
S.C.P. OUT
HD OUT EXT BPP IN
POWER OFF IN YM SW
CUT OFF
RGB OUT
Vcc (9V) GND
Vcc (5V)
Vcc (9V)

**Fig. 5-4**

# 3. CRT OUTPUT CIRCUIT

## 3-1. General

The CRT output circuit is composed of a cascade connection, RGB output circuit using DC bias circuit, white width improvement circuit and a blue extension circuit. As shown in Fig. 5-5, the white width improvement circuit and DC bias circuit are included in the R drive unit and the blue extension circuit in the B drive unit.

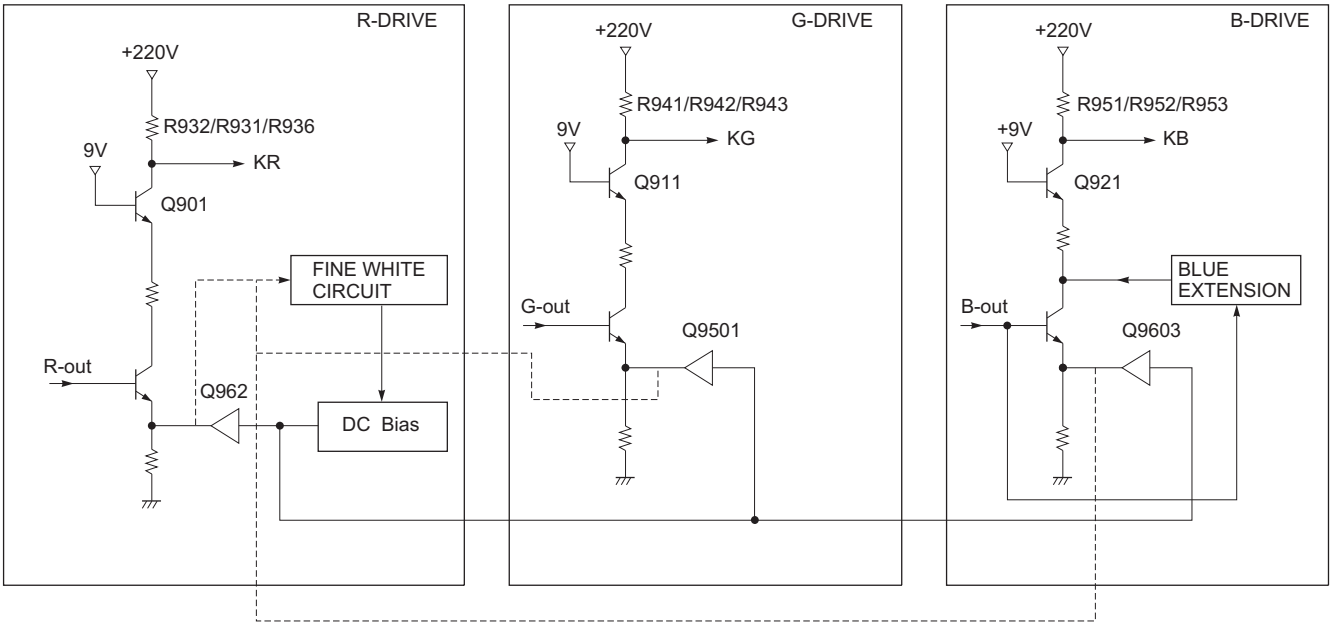



**Fig. 5-5**

## 3-2. Output Circuit

Among the output circuits, R- out circuit is shown in Fig. 5-6. The output transistor Q901 is connected to Q913 in the output is developed at the collector. The DC bias voltage is set to the same voltage level as the emitter voltage of Q913 in the cut off and determines the AC gain. The cutoff voltage is determined by R916, R914 & R931// R932//R936 and the cutoff voltage (R CUTOFF) of R out signal. This is shown by the following equation.

$$V_{CUTOFF} = (220 - R931//R932//R936)\left(\frac{R_{CUTOFF} - 0.7}{R916} - \frac{0.7}{R914}\right)$$

C914, L912 and L913 are used for correcting the frequency response and each operates as a high frequency peaking filter.

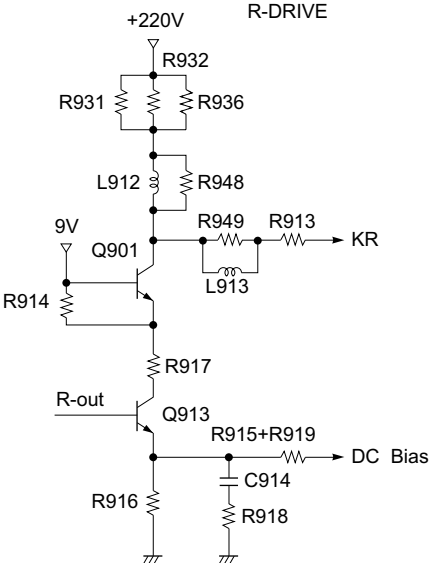



**Fig. 5-6**

## 3-3. Blue Extension Circuit

The blue extension circuit controls Q921 emitter current depending on the B-out level and corrects the B-CRT luminance characteristic, thereby obtaining even white level.

When B-out level rises and the base voltage level of Q9605 exceeds the cut off level specified by the emitter of Q9601, Q9605 turns ON and the gain of Q921 rises. ("B" area in Fig. 5-8)

After that, if the level rises furthermore, Q9602 turns ON and mutes Q9605. ("C" area in Fig. 5-8)

Due to above operations, B-drive input/output characteristics as shown in Fig. 5-8 is obtained.

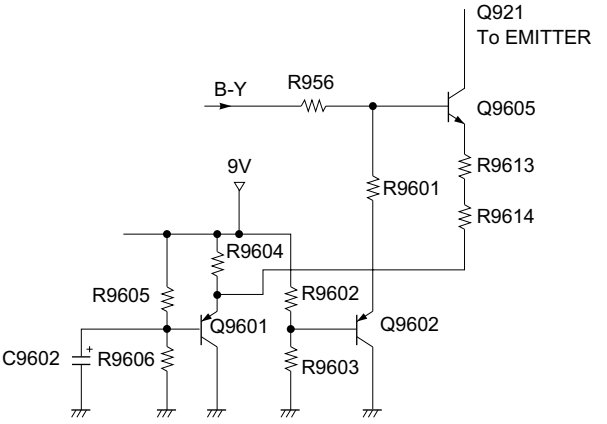



**Fig. 5-7**

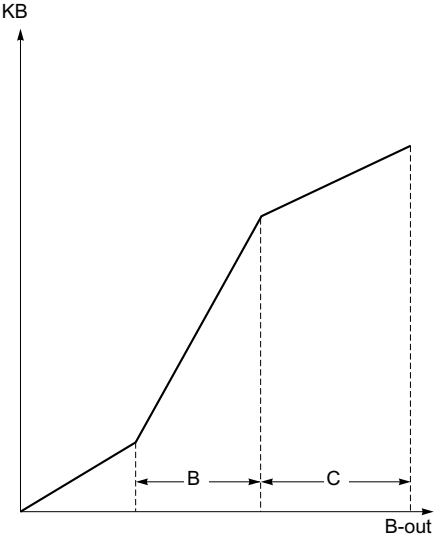



**Fig. 5-8**

# SECTION VI
# YCS/DUAL CIRCUIT

# 1. GENERAL

The YCS/DUAL circuit puts YCS and DUAL on the same PCB to share the memory IC. This circuit comprises the following 3 blocks.

- DUAL block
- YCS block

# 2. OPERATION PRINCIPLE

## 2-1. DUAL Block

This is the circuit to process signals of the subscreen, and has the following functions.

- Compressing the subscreen of the double window to 1/2
- Still picture of subscreen
- 9-screen multi-search
- OSD superimpose (only at 9-screen multi-search)
- Main/sub screen images superimpose with YIQ signal.

## 2-2. YCS (3-dimension YCS Separator) Block

The 3-dimension YCS separator is the comb filter using the frame memory, and separates ideally the bright signal and color signal with respect to a still picture, providing a clean image without:

- Dot disturbance generated at the color BOUNDARY
- Exudation of color in the vertical direction (cross-color)

However, separation fails in the moving picture because the picture moves in the front/rear frames.

The YCS block detects motion, and switches the separation mode: the 2-dimension YC separation using a line memory for a moving picture, and the 3-dimension YC separation for a still picture. These two separation modes compensate each other and result in ideal YC separation.

## 2-3. Memory Selector Block

This selects the memory use state in:

- 2-screen (9-screen): DUAL
- 1-screen: YCS

The switching is controlled with pin 20 of QY03 (MOH) in the DUAL block.

# 3. CIRCUIT OPERATION

Fig. 6-1 shows the block diagram of YCS/DUAL.

## 3-1. DUAL Section

The POP video signal is supplied from pin 8 of PY01, and is applied to pin 4 of QZ100 (DIGITAL COMB). The Y and C signals from pin 15 and 13 are applied to pin 40 (Y IN) and pin 6 (CHROMA IN) of QY01(V/C/D IC) respectively.

The Y, I, Q signals from pin 37, pins 48 and 47 of QY01 are limited in their bands in the LPF which eliminates a folded distortion, and then applied to pin 8 (YIN), pin 14 (IIN), and pin 16 (PIN) of QY03 (TC90A17F) respectively.

The synchronizing signal in the write channel is generated from the VD signal at pin 13 of QY01 and the HD signal at pin 14, and is applied to pins 21 (WVD) and 22 (WHD) of QY03 respectively.

The synchronizing signal in the read channel is supplied from pins Y11 and Y12 of PY01, and is applied to pins 79 (RVD) and 78 (RHD) of QY03 respectively.

The video signal which was converted to digital data is supplied from pins 33 to 40 and pins 42 to 49 of QY03. The RMCK, WMCK, RRST and WRST signals in the clock channel are supplied from pins 69, 27, 68 and 32 respectively. These signals are supplied to the memory of QY06 and QY07.

The digital data from QY06 and QY07 is applied to pins 51 to 58 and pins 59 to 66 of QY03. This signal is also supplied to QZ01. But, the input data is ignored, because the $I^2C$ BUS is set to make the input/output pin of QZ01 high/high impedance and turns off in the three-dimension.

The Y, I and Q signals, the video signal of the subscreen, from pins 96, 98 and 100 of QY03 pass through the LPF which eliminates a clock component, and are applied to pins 29, 30 and 31 of QY01, the main/sub video signal superimposing circuit. The video signal of the main screen is supplied from pins 1, 2 and 3 of PZ01, and is applied to pins 25, 26 and 27 of QY01. The Ys signal, which is the main/sub video signals selector signal, is led from pin 71 of QY03.

The video signal superimposed with the main/sub video signals is generated from pins Y04, Y05 and Y06 of PY01.

The $I^2C$ BUS data from the main microcomputer is supplied from pins DI and DJ of PZ01, and is applied to pins 82 and 83 of QY03.

## 3-2. YCS Section

The video signal from the AV selector is applied to the input terminal (DG). The input video signal is limited in their bands in the LPF which eliminates a folded distortion, and is applied to pin 70 of QZ01.

The video signal, that was converted to digital data, is applied to pins 32 to 39, 47 to 54 of QZ01. The MEMCK, RRST, WEN1, WEN0, REN1 and REN0 signals of the clock channel are applied to pins 30, 41, 42, 43, 44 and 45 respectively. These signals are input to QY06 and QY07 memory via QZ26 (TC74LVX244).

The digital data from QY06 and QY07 is applied to pins 13 to 28 of QZ01. This signal is also supplied to QY03. But, the input data is ignored, because the analog signals (Y, I, Q) of QY03 are muted.

The luminance signal generated at pin 83 of QZ01 is amplified in the LPF which eliminates the clock component, and the gain amplifier, and then it is outputted from the (DC) terminal as a luminance signal.

The color signal generated at pin 71 of QZ01 is eliminated its clock component in the LPF, amplified in the gain amplifier, and outputted from the (DD) terminal as a color signal.

The system clock to perform Y/C separation operation is a signal of 28.6 MHz components (entered pin 98) abstracted from the waveform, which are generated at pin 90 on the crystal oscillation basis connected to pins 5 and 6 of QZ01, through BPF (band pass filter).

The PLL (phase locked loop) control is carried out so that the clock signal is locked to the input video signal.

# 4. TERMINAL DESCRIPTION

## 4-1. PY01

**Table 6-1**

| No. | Signal name, Voltage, etc. |
|---|---|
| Y01 | Main screen period: 0V,<br>Subscreen period: 5V |
| Y02 | 5V at operating |
| Y03 | GND |
| Y04 | Q-signal output |
| Y05 | Y-signal output |
| Y06 | I-signal output |
| Y07 | GND |
| Y08 | POP video input |
| Y09 | POP Y OUT |
| Y10 | GND |
| Y11 | Vertical synchronizing signal, negative polarity, 5V |
| Y12 | Horizontal synchronizing signal, negative polarity, 5V |
| Y13 | POP VD OUT |
| Y14 | PMK (5V ± 0.5V) |
| Y15 | POP C INPUT (0.6V (p-p) at burst) |

## 4-2. PZ01

**Table 6-2**

| No. | Signal name, Voltage, etc. |
|---|---|
| 1 | Main screen Q-signal input |
| 2 | Main screen I-signal input |
| 3 | Main screen Y-signal input |
| 4 | Sandcastle pulse, positive polarity |
| 5 | GND |
| DH | Comb-through, 3.3V |
| DC | Y comb 2V (p-p) |
| DE | +9V±0.5V |
| DD | C comb 0.6V (p-p) at burst |
| DB | GND |
| DG | V-AV 2V (p-p) |
| DA | +5V±0.5V |
| DF | ¾ ¾ |
| DI | $I^2C$ BUS data, 5V |
| DJ | $I^2C$ BUS clock, 5V |

## 4-3. QZ01 (TC90A28F)

**Table 6-3**

| Pin No. | Name | I/O | Function | Pin No. | Name | I/O | Function |
|---|---|---|---|---|---|---|---|
| 1 | CK8 | I | System clock input | 37 | FMO10 | O | Memory data output |
| 2 | MEMHZ | I | Memory Hi-Z control | 38 | FMO9 | O | Memory data output |
| 3 | MUSEMD | I | MUSE control input | 39 | FMO8 | O | Memory data output |
| 4 | VDD | — | 3.3V | 40 | VSS | — | GND |
| 5 | XI | I | X'tal IN | 41 | RRST | O | Memory R/W reset |
| 6 | XO | O | X'tal OUT | 42 | WEN1 | O | Memory write enable 1 |
| 7 | VSS | — | GND | 43 | WEN0 | O | Memory write enable 0 |
| 8 | KILIN | I | Color killer input | 44 | REN1 | O | Memory read enable 1 |
| 9 | ACNOUT | O | $I^2C$ bus I/O control | 45 | REN0 | O | Memory read enable 0 |
| 10 | SCL | I | $I^2C$ bus clock | 46 | VDD | — | 3.3V |
| 11 | SDA | I/O | $I^2C$ bus data | 47 | FMO7 | O | Memory data output |
| 12 | VDD | — | 3.3V | 48 | FMO6 | O | Memory data output |
| 13 | FMI0 | I | Memory data input (LSB) | 49 | FMO5 | O | Memory data output |
| 14 | FMI1 | I | Memory data input | 50 | FMO4 | O | Memory data output |
| 15 | FMI2 | I | Memory data input | 51 | FMO3 | O | Memory data output |
| 16 | FMI3 | I | Memory data input | 52 | FMO2 | O | Memory data output |
| 17 | FMI4 | I | Memory data input | 53 | FMO1 | O | Memory data output |
| 18 | FMI5 | I | Memory data input | 54 | FMO0 | O | Memory data output (LSB) |
| 19 | FMI6 | I | Memory data input | 55 | VSS | — | GND |
| 20 | FMI7 | I | Memory data input | 56 | VDD | — | 3.3V |
| 21 | FMI8 | I | Memory data input | 57 | HREF | O | H reference timing output |
| 22 | FMI9 | I | Memory data input | 58 | VIN | I | Vertical timing input |
| 23 | FMI10 | I | Memory data input | 59 | VCDBUS | O | Serial bus |
| 24 | FMI11 | I | Memory data input | 60 | BLK | O | Blanking timing output |
| 25 | FMI12 | I | Memory data input | 61 | DCCLMP | O | Clamp pulse output |
| 26 | FMI13 | I | Memory data input | 62 | TEST2 | I | Test terminal |
| 27 | FMI14 | I | Memory data input | 63 | TEST1 | I | Test terminal |
| 28 | FMI15 | I | Memory data input (MSB) | 64 | RESET | I | Reset |
| 29 | VSS | — | GND | 65 | VSS | — | GND |
| 30 | MEMCK | O | Clock for memory | 66 | VDD | — | 3.3V |
| 31 | VDD | — | 3.3V | 67 | VSS | — | GND |
| 32 | FMO15 | O | Memory data output (MSB) | 68 | YVR2 | — | A/D reference (for Y) |
| 33 | FMO14 | O | Memory data output | 69 | AVDD | — | 3.3V (analog) |
| 34 | FMO13 | O | Memory data output | 70 | VIDEO IN | I | Composite /Y video input |
| 35 | FMO12 | O | Memory data output | 71 | AVSS | — | GND (analog) |
| 36 | FMO11 | O | Memory data output | 72 | YVR1 | — | A/D reference (for Y) |

| Pin No. | Name | I/O | Function |
|---|---|---|---|
| 73 | BIAS | — | A/D bias (for Y/C) |
| 74 | YVR2 | — | A/D reference (for C) |
| 75 | AVDD | — | 3.3V (analog) |
| 76 | CIN | I | C video input |
| 77 | AVSS | — | GND (analog) |
| 78 | CVR1 | — | A/D reference (for C) |
| 79 | BIAS1C | — | D/A bias 1 (for C) |
| 80 | AVDD | — | 3.3V (analog) |
| 81 | COUT | O | C video output |
| 82 | AVSS | — | GND (analog) |
| 83 | YOUT | O | Y video output |
| 84 | AVDD | — | 3.3V (analog) |
| 85 | BIAS1Y | — | D/A bias 1 (for Y) |
| 86 | VREFYC | I | D/A reference voltage (for Y/C) |
| 87 | BIAS2YC | — | D/A bias 2 (for Y/C) |
| 88 | BIAS1CK | — | D/A bias 1 (for C) |
| 89 | AVSS | — | GND (analog) |
| 90 | CK1 | O | Clock output |
| 91 | AVDD | — | 3.3V (analog) |
| 92 | VREFCK | I | D/A reference (for clock playback) |
| 93 | BIAS2CK | — | D/A bias 2 (for clock playback) |
| 94 | VDD | — | 3.3V |
| 95 | VSS | — | GND |
| 96 | VDD | — | 3.3V |
| 97 | VSS | — | GND (for self bias) |
| 98 | BPF421 | O | 1820 fH abstraction |
| 99 | VDD | — | 3.3V (for self bias) |
| 100 | CKOUT | O | 1820 fH clock output |

# 5. YCS TROUBLESHOOTING

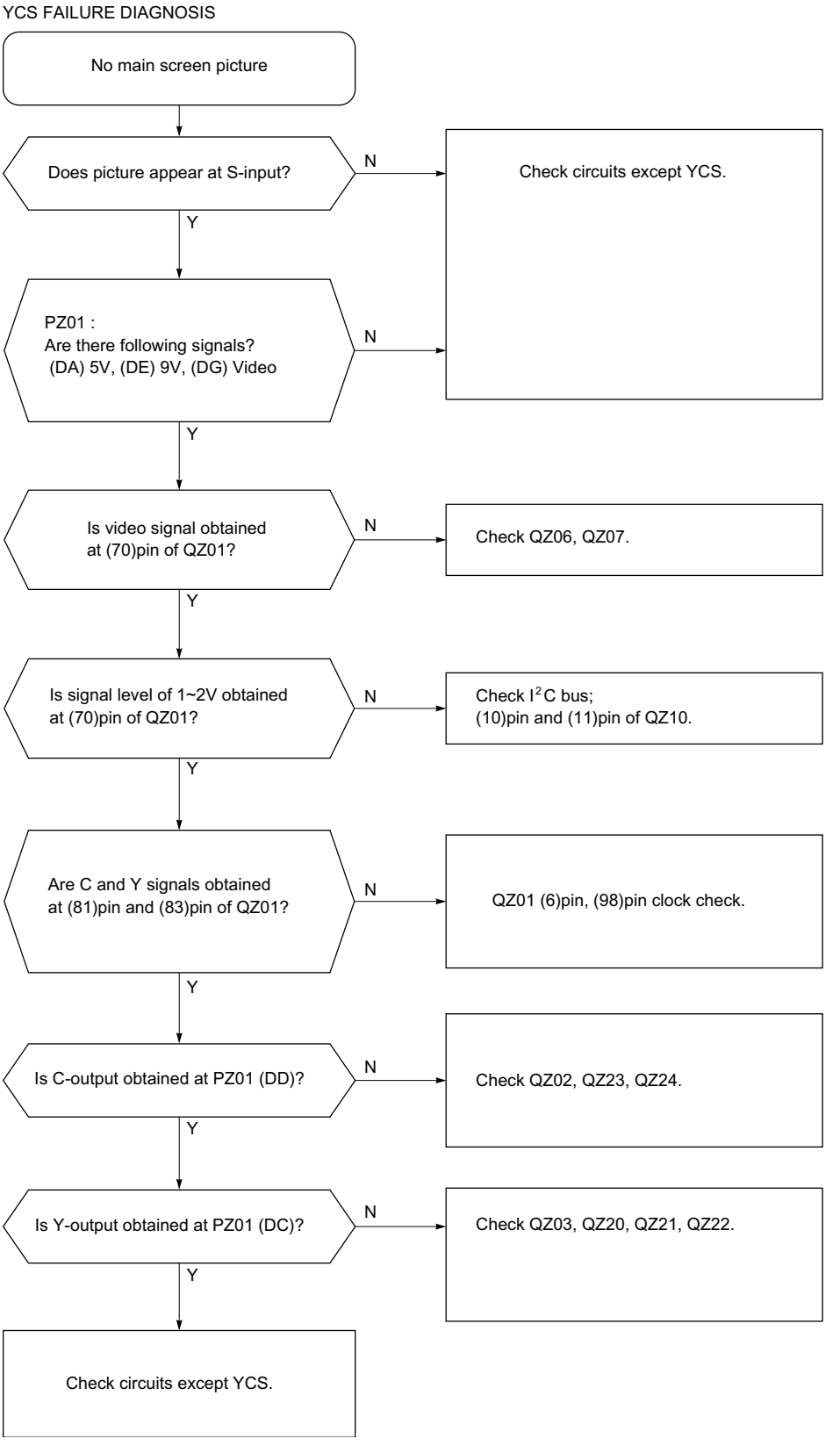



**Fig. 6-1**

# 6. BLOCK DIAGRAM

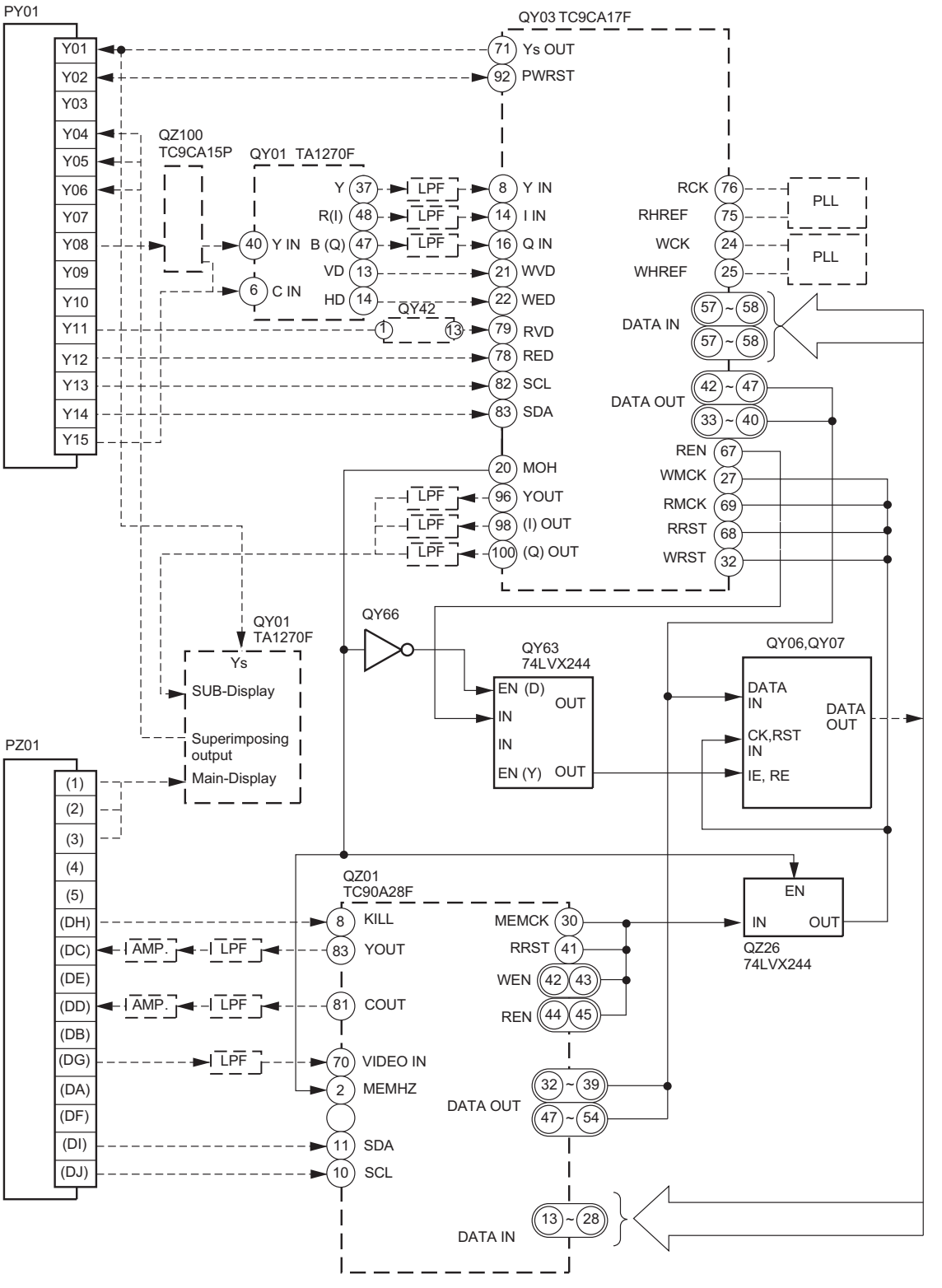



**Fig. 6-2 Block diagram of YCS/DUAL circuit**

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# SECTION VII
# DOUBLE-SPEED CIRCUIT (UPCON)

# 1. GENERAL

The double-speed circuit converts an interlaced scanning frequency signal of approx. 15.75 kHz horizontal frequency in the NTSC system to the progressive scanning signal of motion adaptive type and approx. 31.5 kHz horizontal frequency.

# 2. CIRCUIT OPERATION

## 2-1. Signal Flow

Fig. 7-1 shows the block diagram of this circuit.

### 2-1-1. Input Section

The Y-signal (luminance signal) applied to pin 214 of PX01 is applied to the pin 63 of QX100, A/D converter, through the 6dB amplifier and the low-pass filter. The I and Q signals (color signals) are applied to pins 50 and 31 of QX100 through the amplifier and the low-pass filter, like the Y-signal which is applied to pins 216 and 218 of PX01.

The Y/I/Q signals are clamped in the internal clamp circuit, and are converted to digital signals. The Y-signal is developed from pins 6 to 13 as an 8-bit data, and is applied to QX300. The I/Q signals are 8-bit data that are IQ multiplexed and developed from pins 17 to 24 as a C-signal, and is applied directly to QX400 without passing through QX300.

### 2-1-2. Motion Adaptive Type Progressive Scanning Line Number Conversion Section

The scanning line number changing IC QX300 (SLC) changes the number of scanning lines by applying the Y-signal input at pins 136 to 129 to the built-in line memory and the external field memory of QX310 and QX320.

Detecting the video signal movement, make the still portion fine flicker-free image with vertical resolution by developing the previous field signal, and develops the signal generated from the current filed for the moving portion.

For the Y-signal processed as above, output the interpolation signal processed matching the moving portion and still portion from pins 39 to 42, and output the direct signal which is the input signal to be developed directly as an output from pins 43 to 47. The interpolation and direct output signal are 8-bit 14.3 MHz in the IC, but multiplexed to 4-bit 28.6 MHz in MSB and LSB sides when it is developed.

### 2-1-3. Double-speed Converter Section

The Y/I/Q signals are processed with the double-speed converter/vertical expansion-compression IC QX400 (JFORC), external field memory QX440 and QX450 and the line memory QX460, QX465, QX470 and QX480.

The interpolation and direct Y-signals which were changed in the number of scanning lines are applied to pins 198 to 195 and 192 to 189. The I/Q signals are multiplexed as described above and are applied to pins 209 to 202.

The rate of Y signal is improved from approx. 15.75 kHz horizontal frequency to 31.5 kHz using line memories of QX470 and QX480. Then the switch built-in inside QX400 switches the signal for an interpolation signal and a direct signal and develops on y signal (motion adaptive type progressive scanning signal).

On the other hand, the rate of I and Q signals is improved from approx. 15.75 kHz horizontal frequency to 31.5 kHz using line memories of QX460 and QX465 in the same way as Y signal. Then the same signal is converted into two line signals.

Thus processed Y/I/Q signals are developed as 8-bit data from pins 18 to 11, 42 to 35 and 28 to 21 pins, respectively.

The field memory of QX440 and QX450 is used to match the phase between the developed Y/I/Q signals and output sync system signal.

### 2-1-4. Output Section

The Y/I/Q signals from QX400 are applied to pins 1 to 8, 9 to 16 and 18 to 25 of QX500, the D/A converter, respectively. The Y/I/Q signals which are converted to analog signals in QX500 are developed from pins 40, 38 and 36, respectively, and then they are developed from pin 204, 206 and 208 of PX01, respectively, through the low-pass filter.

## 2-2. Clock/Sync Signal

All the clock signals used in the (a) input section, (b) motion adaptive type progressive scanning line number conversion section, (c) double converter section and (d) output section are generated from HD synchronized with the input video signal. The signals are generated at PLL IC QX210 and its clock frequency is approx. 28.6 MHz.

HD/VD out signals are developed from pins 235 and 234 of QX400 to pins 210 and 212 of PX06 directly. SCP out signal adds a horizontal mask signal at pin 7 of QX400 and a clamp signal which changes the signal width by a mono-stable multi-vibrator QX456. Then the signals are developed from pin 202 of PX01.

VMSK out signal develops from pin 6 of X400 to pin 201 of PX01 directly.

## 2-3. $I^2C$ BUS

Setting of the processing conditions of QX300 and QX400 are controlled by the $I^2C$ BUS clock and data applied to pins 51 and 53 of PX04.

# 3. BLOCK DIAGRAM

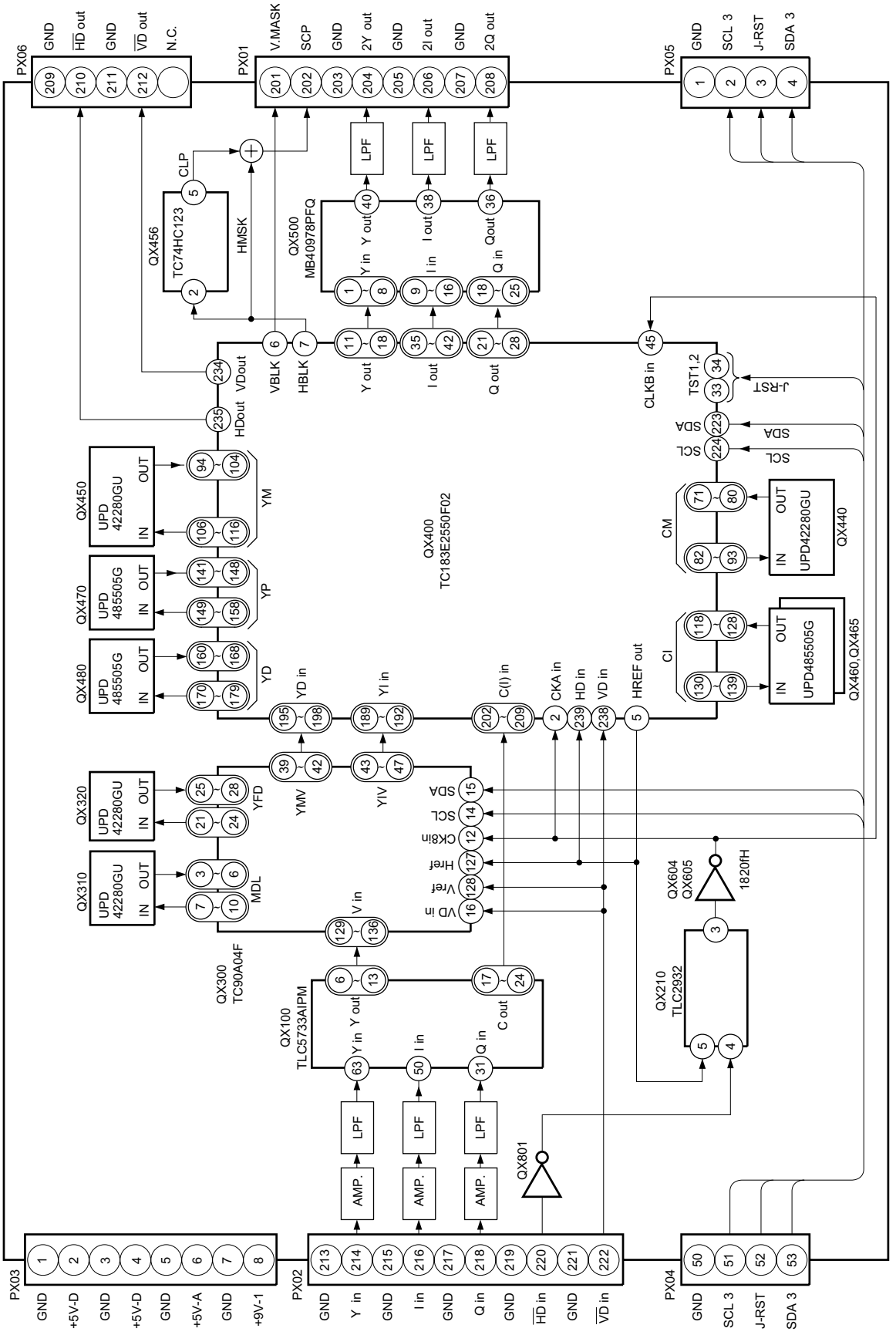


**Fig. 7-1 Block diagram of double-speed circuit (UP CON)**

# 4. PIN ASSIGNMENT

**Table 7-1**

| Pin No. | Signal Name | Buffer name | Type | Pin No. | Signal name | Buffer name | Type | Pin No. | Signal name | Buffer name | Type |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VSS | —— | — | 37 | IOUT2 | B8IF | OUT | 73 | CMIN2 | TLCHTIF | IN |
| 2 | CKAIN | IBUFIF | IN | 38 | IOUT3 | B8IF | OUT | 74 | CMIN3 | TLCHTIF | IN |
| 3 | VDDA | —— | — | 39 | IOUT4 | B8IF | OUT | 75 | CMRE | B8IF | OUT |
| 4 | VMSK | B81F | OUT | 40 | IOUT5 | B8IF | OUT | 76 | CMRR | B8IF | OUT |
| 5 | HREFOUT | B81F | OUT | 41 | IOUT6 | B8IF | OUT | 77 | CMIN4 | TLCHTIF | IN |
| 6 | VBLK | B81F | OUT | 42 | IOUT7 | B8IF | OUT | 78 | CMIN5 | TLCHTIF | IN |
| 7 | HBLK | B81F | OUT | 43 | DAICK | B8IF | OUT | 79 | CMIN6 | TLCHTIF | IN |
| 8 | CLAMP | B81F | OUT | 44 | VDDA | — | — | 80 | CMIN7 | TLCHTIF | IN |
| 9 | VSS | —— | — | 45 | CKBIN | IBUFIF | IN | 81 | VSS | — | — |
| 10 | VDDA | —— | — | 46 | VSS | — | — | 82 | CMOUT7 | B8IF | OUT |
| 11 | YOUT0 | B81F | OUT | 47 | YFIN0 | TLCHTIF | IN | 83 | CMOUT6 | B8IF | OUT |
| 12 | YOUT1 | B81F | OUT | 48 | YFIN1 | TLCHTIF | IN | 84 | CMOUT5 | B8IF | OUT |
| 13 | YOUT2 | B81F | OUT | 49 | YFIN2 | TLCHTIF | IN | 85 | CMOUT4 | B8IF | OUT |
| 14 | YOUT3 | B81F | OUT | 50 | YFIN3 | TLCHTIF | IN | 86 | CMWR | B8IF | OUT |
| 15 | YOUT4 | B81F | OUT | 51 | YFRR | B8IF | OUT | 87 | CMWE | B8IF | OUT |
| 16 | YOUT5 | B81F | OUT | 52 | YFIN4 | TLCHTIF | IN | 88 | CMOUT3 | B8IF | OUT |
| 17 | YOUT6 | B81F | OUT | 53 | YFIN5 | TLCHTIF | IN | 89 | CMOUT2 | B8IF | OUT |
| 18 | YOUT7 | B81F | OUT | 54 | YFIN6 | TLCHTIF | IN | 90 | VDDB | — | — |
| 19 | DAYCK | B81F | OUT | 55 | YFIN7 | TLCHTIF | IN | 91 | VSS | — | — |
| 20 | VSS | —— | — | 56 | VDDA | — | — | 92 | CMOUT1 | B8IF | OUT |
| 21 | QOUT0 | B81F | OUT | 57 | VSS | — | — | 93 | CMOUT0 | B8IF | OUT |
| 22 | QOUT1 | B81F | OUT | 58 | YFOUT7 | B8IF | OUT | 94 | YMIN0 | TLCHTIF | IN |
| 23 | QOUT2 | B81F | OUT | 59 | YFOUT6 | B8IF | OUT | 95 | YMIN1 | TLCHTIF | IN |
| 24 | QOUT3 | B81F | OUT | 60 | VDDA | — | — | 96 | YMIN2 | TLCHTIF | IN |
| 25 | QOUT4 | B81F | OUT | 61 | VSS | — | — | 97 | YMIN3 | TLCHTIF | IN |
| 26 | QOUT5 | B81F | OUT | 62 | YFOUT5 | B8IF | OUT | 98 | YMRE | B8IF | OUT |
| 27 | QOUT6 | B81F | OUT | 63 | YFOUT4 | B8IF | OUT | 99 | YMRR | B8IF | OUT |
| 28 | QOUT7 | B81F | OUT | 64 | YFWR | B8IF | OUT | 100 | VDDA | — | — |
| 29 | DAQCK | B81F | OUT | 65 | YFWE | B8IF | OUT | 101 | VSS | — | — |
| 30 | VDDB | —— | — | 66 | YFOUT3 | B8IF | OUT | 102 | YMIN4 | TLCHTIF | IN |
| 31 | VSS | —— | — | 67 | YFOUT2 | B8IF | OUT | 103 | YMIN5 | TLCHTIF | IN |
| 32 | TEST0 | IBUFIF | IN | 68 | YFOUT1 | B8IF | OUT | 104 | YMIN6 | TLCHTIF | IN |
| 33 | TEST1 | IBUFIF | IN | 69 | YFOUT0 | B8IF | OUT | 105 | YMIN7 | TLCHTIF | IN |
| 34 | TEST2 | IBUFIF | IN | 70 | VDDA | — | — | 106 | YMOUT7 | B8IF | OUT |
| 35 | IOUT0 | B8IF | OUT | 71 | CMIN0 | TLCHTIF | IN | 107 | YMOUT6 | B8IF | OUT |
| 36 | IOUT1 | B8IF | OUT | 72 | CMIN1 | TLCHTIF | IN | 108 | YMOUT5 | B8IF | OUT |

| Pin No. | Signal Name | Buffer name | Type | Pin No. | Signal name | Buffer name | Type | Pin No. | Signal name | Buffer name | Type |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 109 | YMOUT4 | B8IF | OUT | 145 | YPIN3 | TLCHTIF | IN | 181 | VSS | — | — |
| 110 | VDDA | —— | — | 146 | YPIN2 | TLCHTIF | IN | 182 | A04M3WR | B8IF | OUT |
| 111 | YMWR | B8IF | OUT | 147 | YPIN1 | TLCHTIF | IN | 183 | A04M3WE | B8IF | OUT |
| 112 | YMWE | B81F | OUT | 148 | YPIN0 | TLCHTIF | IN | 184 | A04M3RR | B8IF | OUT |
| 113 | YMOUT3 | B81F | OUT | 149 | YIOUT0 | B81F | OUT | 185 | A04M2WR | B8IF | OUT |
| 114 | YMOUT2 | B81F | OUT | 150 | VDDB | — | — | 186 | A04M2WE | B8IF | OUT |
| 115 | YMOUT1 | B81F | OUT | 151 | VSS | — | — | 187 | A04M2RR | B8IF | OUT |
| 116 | YMOUT0 | B81F | OUT | 152 | YIOUT1 | B81F | OUT | 188 | VDDA | — | — |
| 117 | VSS | — | — | 153 | YIOUT2 | B81F | OUT | 189 | YIIN0 | IBUFIF | IN |
| 118 | CIN7 | TLCHTIF | IN | 154 | YIOUT3 | B81F | OUT | 190 | YIIN1 | IBUFIF | IN |
| 119 | CIN6 | TLCHTIF | IN | 155 | YIOUT4 | B81F | OUT | 191 | YIIN2 | IBUFIF | IN |
| 120 | VDDA | — | — | 156 | YIOUT5 | B81F | OUT | 192 | YIIN3 | IBUFIF | IN |
| 121 | VSS | — | — | 157 | YIOUT6 | B81F | OUT | 193 | VSS | — | — |
| 122 | CIN5 | TLCHTIF | IN | 158 | YIOUT7 | B81F | OUT | 194 | VDDA | — | — |
| 123 | CIN4 | TLCHTIF | IN | 159 | VDDA | — | — | 195 | YDIN0 | IBUFIF | IN |
| 124 | CLRR | B8IF | OUT | 160 | YPDIN7 | TLCHTIF | IN | 196 | YDIN1 | IBUFIF | IN |
| 125 | CIN3 | TLCHTIF | IN | 161 | YPDIN6 | TLCHTIF | IN | 197 | YDIN2 | IBUFIF | IN |
| 126 | CIN2 | TLCHTIF | IN | 162 | YPDIN5 | TLCHTIF | IN | 198 | YDIN3 | IBUFIF | IN |
| 127 | CIN1 | TLCHTIF | IN | 163 | YPDIN4 | TLCHTIF | IN | 199 | VSS | — | — |
| 128 | CIN0 | TLCHTIF | IN | 164 | YLRR | B81F | OUT | 200 | NANDOUT | B41F | OUT |
| 129 | VDDA | — | — | 165 | YPDIN3 | TLCHTIF | IN | 201 | TSTCK4 | IBUFIF | IN |
| 130 | CIOUT0 | B8IF | OUT | 166 | YPDIN2 | TLCHTIF | IN | 202 | IIN0 | IBUFIF | IN |
| 131 | CIOUT1 | B8IF | OUT | 167 | YPDIN1 | TLCHTIF | IN | 203 | IIN1 | IBUFIF | IN |
| 132 | CIOUT2 | B8IF | OUT | 168 | YPDIN0 | TLCHTIF | IN | 204 | IIN2 | IBUFIF | IN |
| 133 | CIOUT3 | B8IF | OUT | 169 | VSS | — | — | 205 | IIN3 | IBUFIF | IN |
| 134 | CLDRST | B8IF | OUT | 170 | YDOUT0 | B81F | OUT | 206 | IIN4 | IBUFIF | IN |
| 135 | CLWCK | B8IF | OUT | 171 | YDOUT1 | B81F | OUT | 207 | IIN5 | IBUFIF | IN |
| 136 | CIOUT4 | B8IF | OUT | 172 | YDOUT2 | B81F | OUT | 208 | IIN6 | IBUFIF | IN |
| 137 | CIOUT5 | B8IF | OUT | 173 | YDOUT3 | B81F | OUT | 209 | IIN7 | IBUFIF | IN |
| 138 | CIOUT6 | B8IF | OUT | 174 | YLWR | B81F | OUT | 210 | VDDB | — | — |
| 139 | CIOUT7 | B8IF | OUT | 175 | YLWCK | B81F | OUT | | | | |
| 140 | VSS | — | — | 176 | YDOUT4 | B81F | OUT | | | | |
| 141 | YPIIN7 | TLCHTIF | IN | 177 | YDOUT5 | B81F | OUT | | | | |
| 142 | YPIIN6 | TLCHTIF | IN | 178 | YDOUT6 | B81F | OUT | | | | |
| 143 | YPIIN5 | TLCHTIF | IN | 179 | YDOUT7 | B81F | OUT | | | | |
| 144 | YPIIN4 | TLCHTIF | IN | 180 | VDDA | — | — | | | | |

| Pin No. | Signal name | Buffer name | Type |
|---|---|---|---|
| 211 | VSS | — | — |
| 212 | QIN0 | IBUFIF | IN |
| 213 | QIN1 | IBUFIF | IN |
| 214 | QIN2 | IBUFIF | IN |
| 215 | QIN3 | IBUFIF | IN |
| 216 | QIN4 | IBUFIF | IN |
| 217 | QIN5 | IBUFIF | IN |
| 218 | QIN6 | IBUFIF | IN |
| 219 | QIN7 | IBUFIF | IN |
| 220 | VDDB | — | — |
| 221 | VSS | — | — |
| 222 | IBDR | IBUFIF | IN |
| 223 | SDA | BD4CODIF | BID |
| 224 | SCL | SMTCIF | IN |
| 225 | POWOFF | IBUFIF | IN |
| 226 | ADD0 | IBUFIF | IN |
| 227 | ADD1 | IBUFIF | IN |
| 228 | ADD2 | IBUFIF | IN |
| 229 | ADD3 | IBUFIF | IN |
| 230 | ADD4 | IBUFIF | IN |
| 231 | ADD5 | IBUFIF | IN |
| 232 | ADD6 | IBUFIF | IN |
| 233 | VDDA | — | — |
| 234 | VDOUT | B81F | OUT |
| 235 | HDOUT | B81F | OUT |
| 236 | ADCLP | B81F | OUT |
| 237 | VSS | — | — |
| 238 | VDIN | IBUFIF | IN |
| 239 | HDIN | IBUFIF | IN |
| 240 | VDDA | — | — |

# 5 . TERMINAL DESCRIPTION AND TROUBLESHOOTING

**Table 7-2**

| Connector No. | Pin No. | Terminal name | Signal name | Voltage, etc. | No power supply | No Y output | Abnormal Contrast | No color output | Abnormal color signal | Screen noise | Wavering screen |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PX01 | 201 | V. MASK | V mask pulse output | 5V, positive polarity | | | | | | | |
| | 202 | SCP | Clamp/ mask | 4.3V/2.0V | | | | | | | |
| | 203 | GND | GND | 0V | | | | | | | |
| | 204 | 2YOUT | Doubld speed Y signal output | 1V(p-p) | | O | O | | | O | |
| | 205 | GND | GND | 0V | | | | | | | |
| | 206 | 2IOUT | Double speed I signal output | 1V(p-p) | | | | O | O | O | |
| | 207 | GND | GND | 0V | | | | | | | |
| | 208 | 2QOUT | Double speed Q signal output | 1V(p-p) | | | | O | O | O | |
| PX02 | 213 | GND | GND | 0V | | | | | | | |
| | 214 | Y IN | Y signal input | 1V(p-p) | | O | O | | | O | |
| | 215 | GND | GND | 0V | | | | | | | |
| | 216 | I IN | I signal input | 1V(p-p) | | | | O | O | O | |
| | 217 | GND | GND | 0V | | | | | | | |
| | 218 | Q IN | Q signal input | 1V(p-p) | | | | O | O | O | |
| | 219 | GND | GND | 0V | | | | | | | |
| | 220 | $\overline{\text{HD}}$ IN | HD signal input | 5V, negative polarity | | | | | | | O |
| | 221 | GND | GND | 0V | | | | | | | |
| | 222 | $\overline{\text{VD}}$ IN | VD signal input | 5V, negative polarity | | | | | | | O |
| PX03 | 1 | GND | GND | 0V | | | | | | | |
| | 2 | +5V – D | +5V power supply | +5V, ±0.25V | O | O | O | O | O | O | O |
| | 3 | GND | GND | 0V | | | | | | | |
| | 4 | +5V – D | 5V power supply | +5V, ±0.25V | O | O | O | O | O | O | O |
| | 5 | GND | GND | 0V | | | | | | | |
| | 6 | +5V – A | 5V power supply | +5V, ±0.25V | O | O | O | O | O | O | O |
| | 7 | GND | GND | 0V | | | | | | | |
| | 8 | +9V – 1 | 9V power supply | +9V, ±0.5V | O | O | O | O | O | O | O |
| PX04 | 50 | GND | GND | 0V | | | | | | | |
| | 51 | SCL2 | $I^2C$ bus clock | 5V | | O | O | O | O | O | O |
| | 52 | J-RST | J-RESET | 0V | | O | O | O | O | O | O |
| | 53 | SDA2 | $I^2C$ bus data | 5V | | O | O | O | O | O | O |
| PX05 | 1 | GND | GND | 0V | | | | | | | |
| | 2 | SCL2 | $I^2C$ bus clock | 5V | | O | O | O | O | O | O |
| | 3 | J-RST | J-RESET | 0V | | O | O | O | O | O | O |
| | 4 | SDA2 | $I^2C$ bus data | 5V | | O | O | O | O | O | O |

| Connector No. | Pin No. | Terminal name | Signal name | Voltage, etc. | No power supply | No Y output | Abnormal Contrast | No color output | Abnormal color signal | Screen noise | Wavering screen |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PX06 | 209 | GND | GND | 5V, negative polarity | | | | | | | |
| | 210 | $\overline{\text{HD}}$ OUT | HD signal output | 0V | | | | | | | O |
| | 211 | GND | GND | 0V | | | | | | | |
| | 212 | $\overline{\text{VD}}$ OUT | VD signal output | 5V, negative polarity | | | | | | | O |
| | | N.C. | Not connected. | ———— | | | | | | | |

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# SECTION VIII
# SYNC SEPARATION CIRCUIT &
# HORIZONTAL OSCILLATION CIRCUIT

# 1. OUTLINE

The horizontal oscillation circuit in the model of this series differs from the usual PJTV models because the progressive scan system is employed.

The signal flow of the sync signal also differs from the usual PJTV models. The signal flow is shown in Fig. 8-1.

As shown in Fig. 8-1, the sync separation circuit uses the built-in circuits inside V/C/D IC (TA1259AN) as in the conventional PJTVs. In this series, the horizontal oscillation circuit additionally employs Q420 (LA7860). This is why the V/C/D IC does not have a function to operate in 2 $f_H$. The next paragraph describes the sync signal flow.

First, for the vertical sync signal, the extracted signal in the sync separation circuit inside V/C/D IC inputs to the up-converter. In the up-converter, the vertical sync signal applied is used as a trigger and another sync signal is created and applied through pin 222.

The phase of the vertical sync signal generated in the up-converter can be delayed to sync signal added from V/C/D IC. The delay amount is controlled when changing the vertical screen position in the zoom mode of a wide model.

On the other hand, the horizontal sync signal, the sync separation circuit built-in V/C/D IC separates to extract a sync signal from the composite video signal. The sync signal is supplied to the AFC circuit inside the IC, then used to control the frequency of the oscillation circuit oscillating with 32 $f_H$ inside the IC. The pulse generated by counting down the pulse of the oscillation circuit inside the IC is supplied to the up-converter as a horizontal sync signal.

In the up-converter, the internal clock is synchronized by using the horizontal sync signal. Here, 2 $f_H$ horizontal sync signal is generated and supplied to IC (LA7860). This is the signal flow of the horizontal sync signal.

The operation principles are shown in the following.

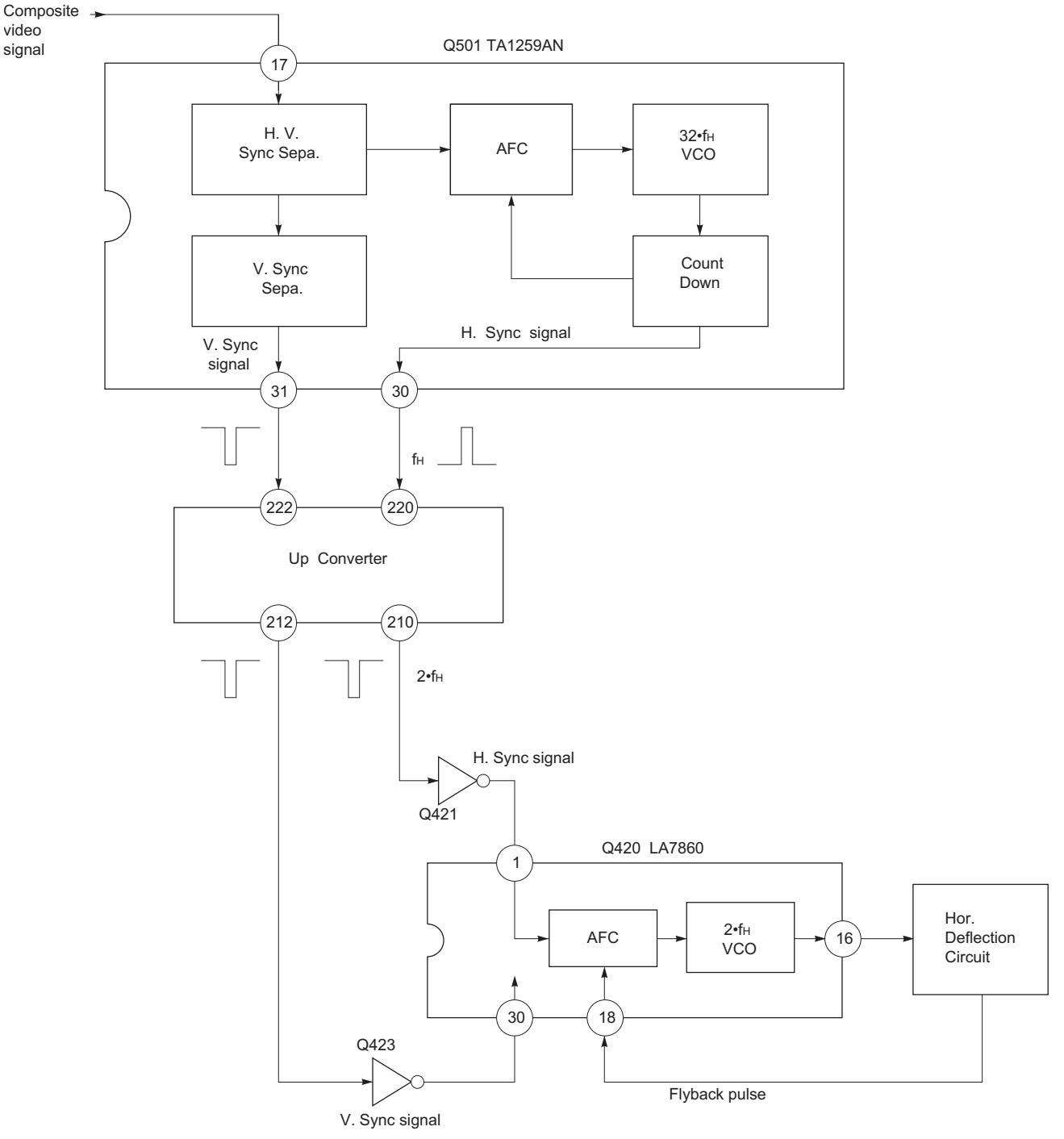



**Fig. 8-1 Sync signal flow**

# 2. SYNC SEPARATION CIRCUIT AND 32 $f_H$ OSCILLATOR

The sync separation circuit separates a sync signal from a video signal and feeds it to an horizontal and vertical deflection circuits.

The separation circuit consists of an amplitude separation (horizontal and vertical sync separation circuit) and a frequency separation circuit (vertical sync separation circuit) which performs the separation by using a frequency difference between horizontal and vertical.

In current chassis, all these sync separation circuits are contained in a V/C/D IC.

Fig. 8-2 shows a block diagram of the sync separation circuit.

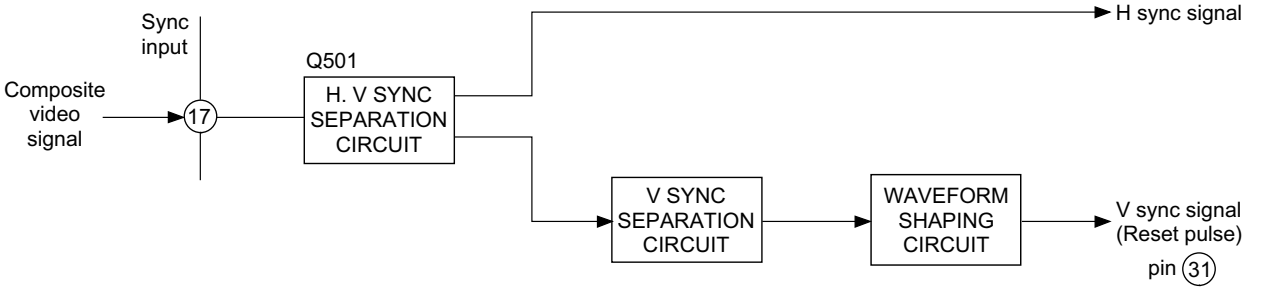



**Fig. 8-2 Sync separation circuit block diagram**

## 2-1. Theory of Operation

### 1-1-1. Auto Slicer Type Sync Separation Circuit

When a sync signal is separated, sync separation is made from the painted end with constant voltage in the old sync separation circuit. The auto slider type circuit employed in this time makes sync separation at a constant rate against the sync signal amplitude. (See Fig. 8-3)

In this method, even if an abnormal signal with small amplitude is applied, stable sync performance can be obtained without separating pedestal.

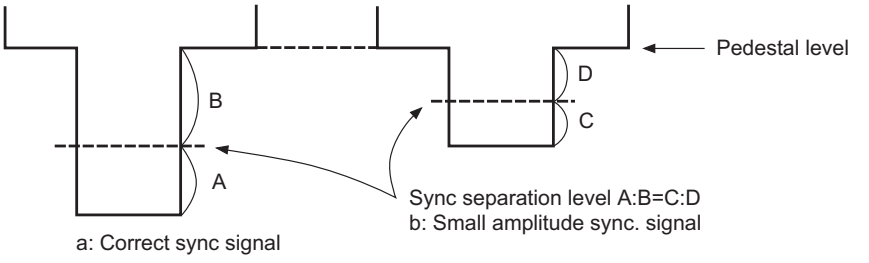



**Fig. 8-3 Sync separation by auto slider system**

### 2-1-2. Vertical Sync Separation Circuit

To separate a vertical sync signal from the composite sync signal consisting of vertical and horizontal sync signals mixed, two stages of integration circuits are provided inside the IC. The circuit consists of a differential circuit and a Miller integration circuit, and has following functions.

(1) Removes horizontal sync signal component.

(2) Maintain stable vertical sync performance for a tape recorded with a copy guard.

(3) Stabilized vertical sync performance under special field conditions (poor field, ghost, sync depressed, adjacent channel best).

The vertical sync signal separated in this stage is processed in a waveform shape circuit.

### 2-1-3. 32 $f_H$ Oscillator

The horizontal sync signal extracted in the sync separation circuit is used in the AFC circuit to control a frequency of the 32 $f_H$ oscillator built-in the IC (Q501).

In the AFC circuit, the output pulse of the 32 $f_H$ oscillator is divided by a divider to stabilize and then supplied to the AFC circuit previously stated. The pulse synchronised with the horizontal scanning frequency $f_H$ divided is supplied to the up-converter circuit in the next stage as a horizontal sync signal.

So, the sync pulse does not include an equalizing pulse with its period in half, but the period is always constant.

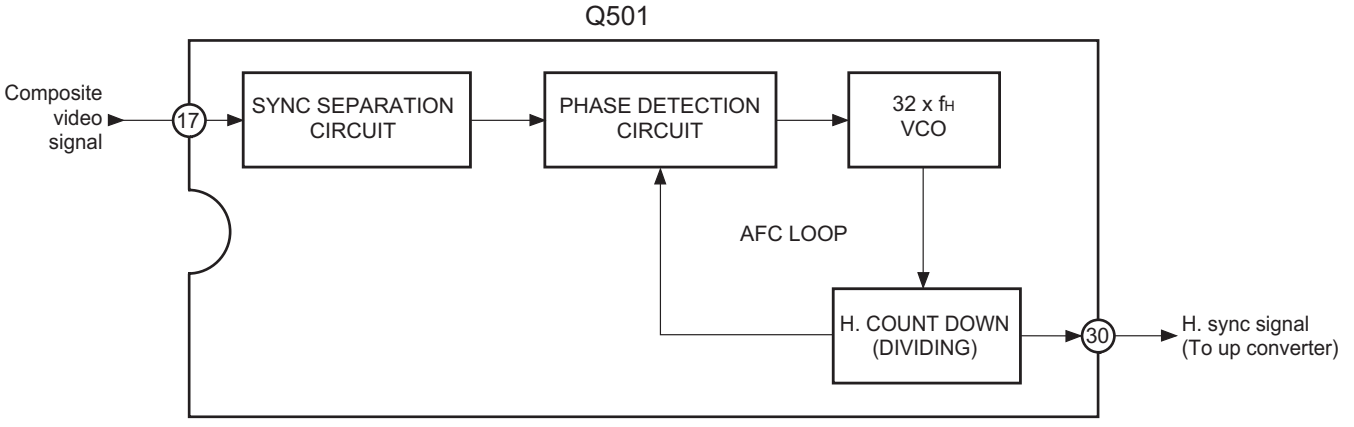



**Fig. 8-4 32 fH oscillator block diagram**

## 3. HORIZONTAL AND VERTICAL OSCILLATION CIRCUIT

As previously stated, the usual PJTV uses the horizontal and vertical oscillation circuits built-in V/C/D IC.

In this model, the horizontal scanning frequency of 31.5 kHz, twice as much as the usual one, is used, so the built-in oscillation circuit cannot be used.

To solve this problem, IC (LA7860) is added. The horizontal and vertical sync signals are supplied to the IC from the up-converter. The up-converter includes a function to change the phase of these sync signals and this function is utilized to perform the screen position adjustment.

As for the data to change the phase in both horizontal and vertical direction, the values selected in designing are entered.

When the screen is scrolled in the zoom mode of the wide model, the phase of the horizontal sync signal is changed by this function and the vertical screen position is moved.

## 3-1. IC (LA7860) Operation

Each pin function and internal operation for the IC (LA7860) is described below. Fig. 8-5 shows a block diagram inside the IC and also shows a circuit of electrical characteristic when measured.

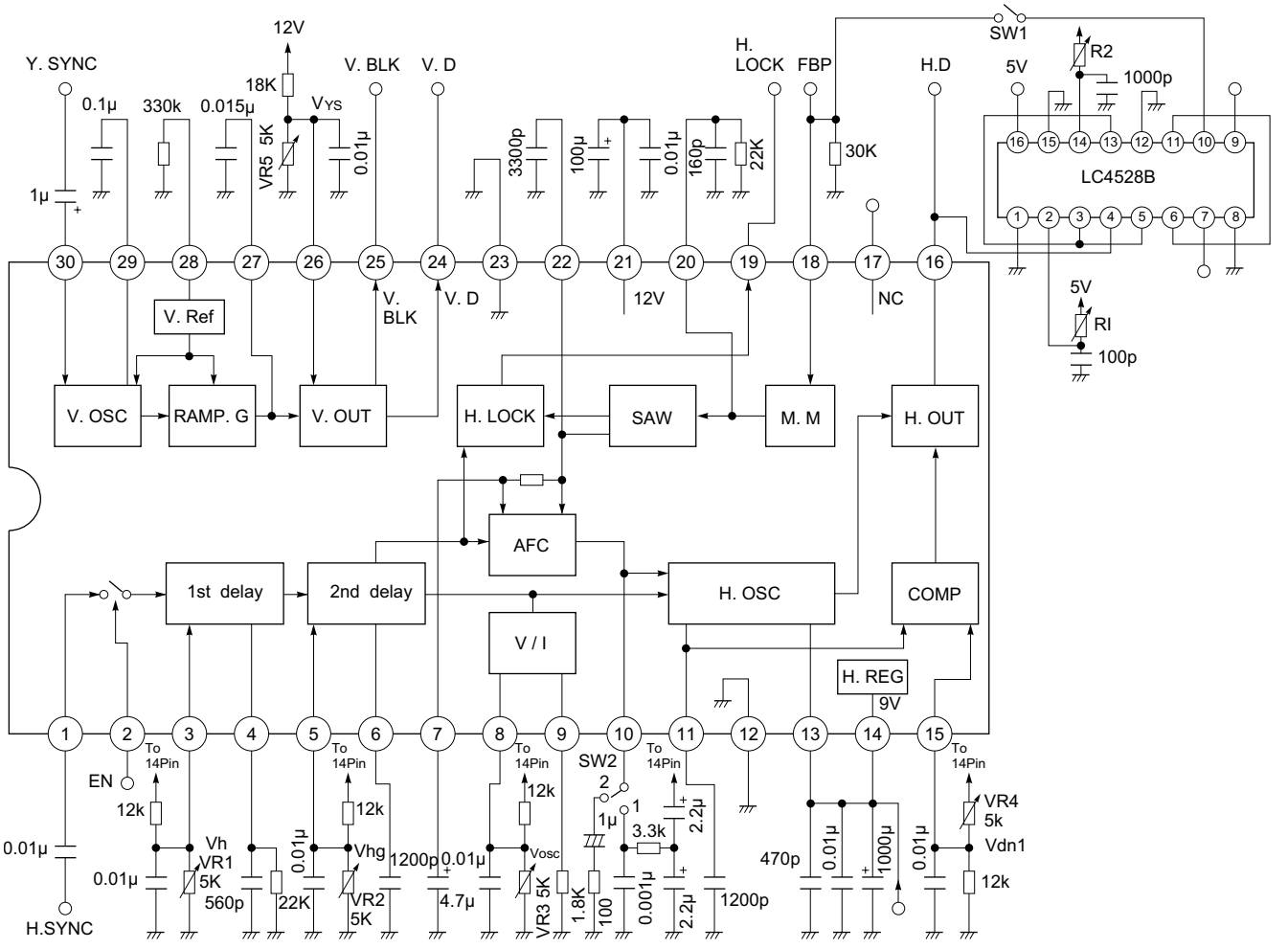



**Fig. 8-5 Electrical characteristic measuring circuit diagram**

(1) Pin 1 is input terminal of horizontal sync signal.

Coupling capacitor of 0.01 mF is used to feed horizontal sync signal of approx. 2V. For input sync signal, both polarities of positive and negative can be allowed, and trigger is done on the front edge.

The pulse width of sync signal which can be input into this terminal, is 3/20 Th (Th:one cycle of horizontal) or less for both polarities of positive and negative.

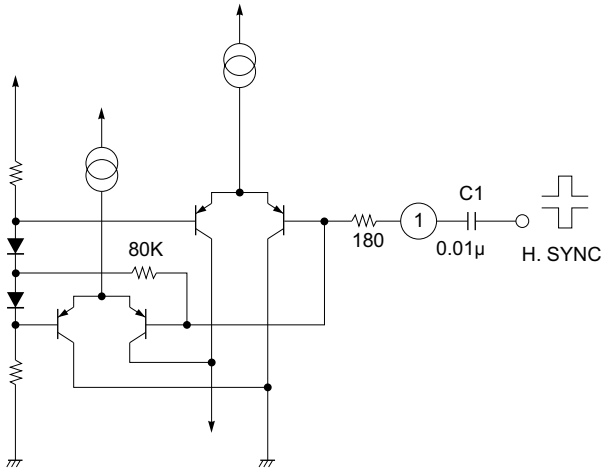



**Fig. 8-6**

(2) Pin 2 is ENABLE terminal of horizontal sync signal.

When this terminal is open, voltage of this terminal turns LOW condition by inside bias of IC.

At the time, horizontal OSC circuit is locked on horizontal sync signal which is input from pin 1.

To turn horizontal OSC circuit to free running condition, the voltage of this terminal is raised to 3V or more.

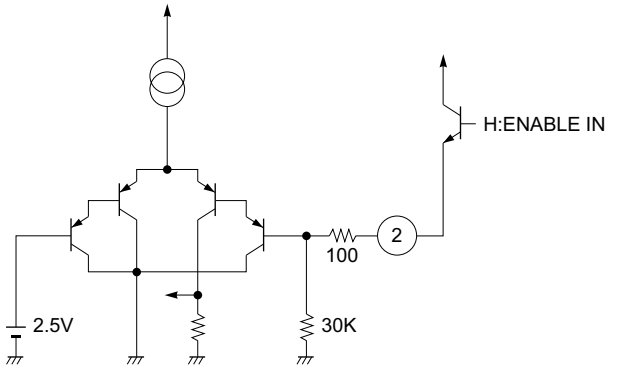



**Fig. 8-7**

(3) Pin 3 is control terminal of H. SHIFT.

Range of control voltage is 0 to 2.5V. When control voltage is 2.5V, phase of FBP becomes most delayed condition to horizontal sync signal.

The horizontal phase shift controlled by this terminal is decided by time constant connected to pin 4, and is independent of horizontal OSC frequency of pin 11.

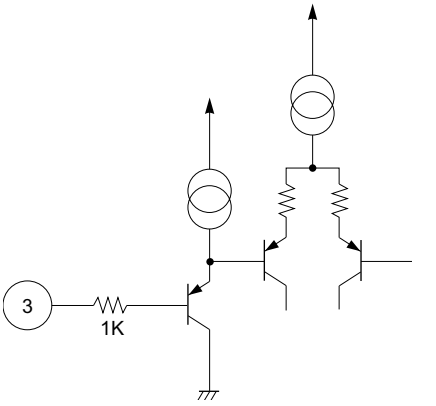



**Fig. 8-8**

(4) Pin 4 is time constant circuit to decide horizontal phase shift controlled by voltage of pin 3.

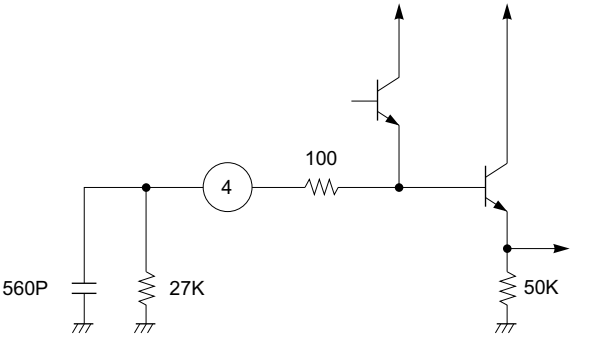



**Fig. 8-9**

(5) Pin 5 is terminal of SHIFT GAIN CONTROL.

Range of control voltage is 0 to 2.5V. When control voltage is 2.5V, phase of FBP becomes most delayed condition to horizontal sync signal. The horizontal phase shift controlled by this terminal is decided by time constant connected to pin 6. And since phase control by this terminal synchronizes to horizontal OSC frequency and uses the same value of capacitor as that connected to pin 6 and 11.

On the assumption that FBP width which is input to pin 18 always constant, when voltage of this terminal is turned to 0V, phase difference does not change with the change of horizontal OSC frequency.

And when the voltage of this terminal is turned to 2.5V, phase of FBP is controlled to the delayed tendency comparing to horizontal OSC frequency input at pin 1. Longer the period of horizontal OSC frequency is, more delayed to the tendency is.

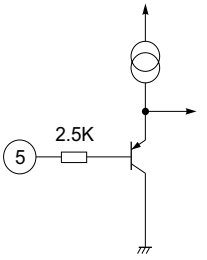



**Fig. 8-10**

(6) Time constant of pin 6 decides the phase shift controlled by pin 5.

Ts is decided by the external time constant at pin 4, and is the first delay value controlled by DC voltage of pin 3. This phase value is not independent of horizontal period. Tg is decided by capacitor at pin 6 and resistor at pin 9, and is the second delay value that is controller by DC voltage of pin 5. This phase value is the function of horizontal period.

Tf is delay value of FBP which is decided by time constant of pin 20.

SAW, which is AFC comparing waveform produced at pin 22, begins discharge from edge of descent.

In Fig. 8-12, $T_{delay}$ means phase value from the front edge of horizontal sync signal input at pin 1, to the center of FBP input to pin 18. In figure, INT. SYNC is made by comparing triangle wave of the second delay with a certain voltage.

The pulse width of INT. SYNC is always 1/10Th, independent of control voltage at pins 3 and 5. Inside IC, the center of INT. SYNC and such a point that 1/10Th passes from the start time of discharge of SAW waveform, are controlled to be coincide together by the AFC circuit.

The control voltage of pin 8 and the horizontal free-running frequency $f_H$ are represented by the following expression.

$f_H=(2/3)\bullet 1/(11.5CR)\bullet(V8+1)$

Here;

V8: Control voltage of pin 8

C: External capacitor of pin 11

R: External resistor of pin 9

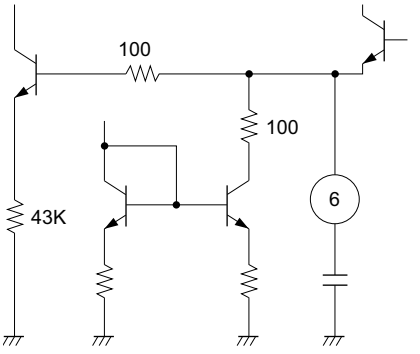



**Fig. 8-11**

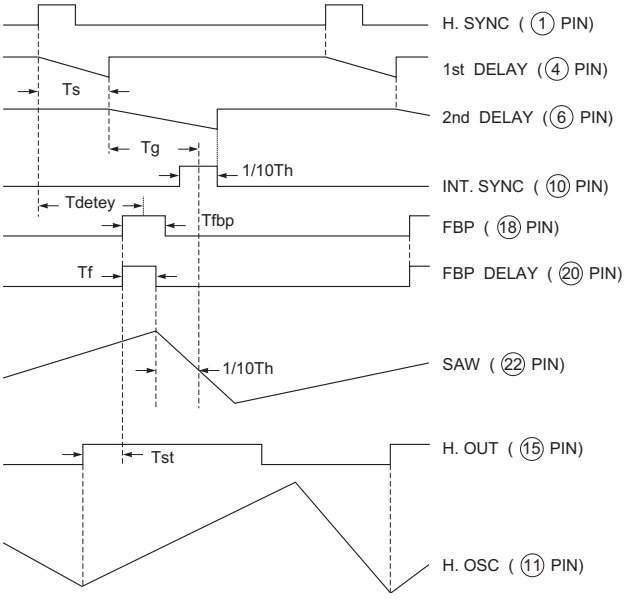



**Fig. 8-12 Timing chart of horizontal phase control**

(7) Pin 7 is connected with capacitor which smooths AFC comparing waveform.

In figure, Vsig is the same signal as the comparing waveform made at pin 22.

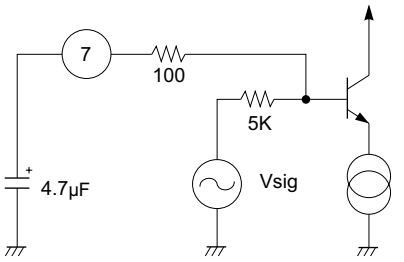



**Fig. 8-13**

(8) Pin 8 is control terminal of horizontal OSC frequency of pin 11.

The range of control voltage is 0 to 2.5V. When this voltage is 0V, horizontal OSC frequency becomes the lowest frequency, and when 2.5V, it becomes maximum.

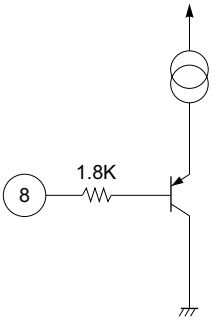



**Fig. 8-14**

(9) Pin 9 gives output of voltage which is added by 1V to the voltage input at pin 8.

The current decided by external resistor flows through horizontal OSC circuit, second DELAY, and SAW generator to control them. Variable resistor RH25 adjusts horizontal OSC frequency.

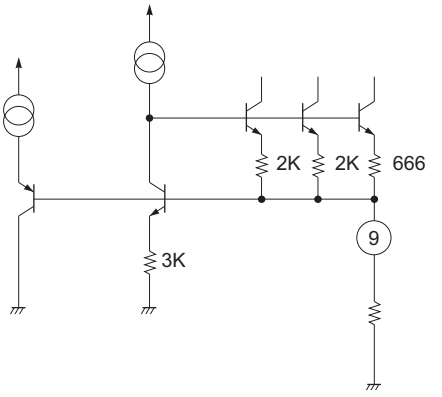



**Fig. 8-15**

(10) Pin 10 is filter terminal of AFC.

The time constant of this filter affects horizontal jitter. The pull-in range of AFC is ±4.7%, and does not depend on the constant of the filter so much.

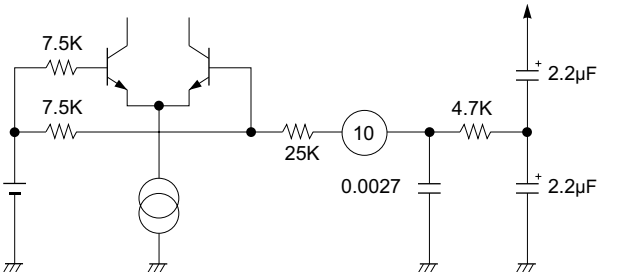



**Fig. 8-16**

(11) Pin 11 is to be connected with horizontal OSC capacitor.

When shifting control range of frequency to upper or lower, the value of capacitor is changed as requested.

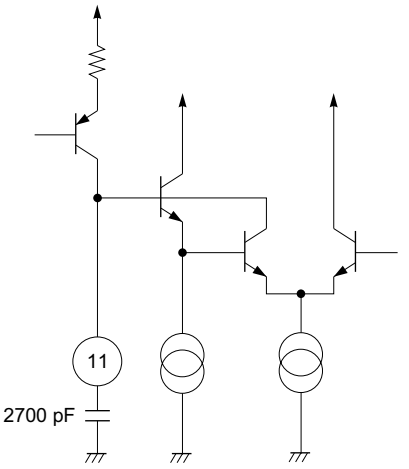



**Fig. 8-17**

(12) Pin 12 is GND terminal of horizontal block.

(13) Pin 13 is a low pass filter giving band limit to horizontal OSC circuit.

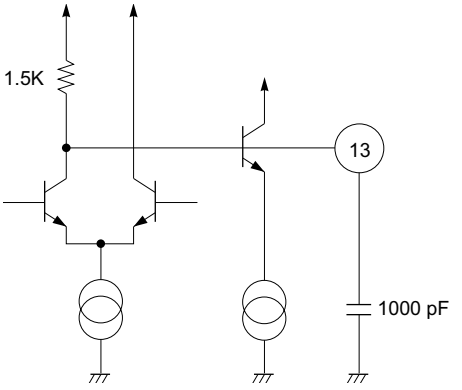



**Fig. 8-18**

(14) Pin 14 is Vcc terminal of horizontal block.

Since pin 14 has approx. 9V regulator inside IC, current of approx. 60 mA is applied at this pin.

(15) Pin 15 is control terminal of H. OUT DUTY.

Controlling the voltage at this terminal from 9V to approx. 7.5V makes possible to regulate the DUTY of H. OUT. The controlling range is approx. 28% to 66% DUTY of H. OUT, when DC voltage of pin 15 is fixed, is always kept constant even though horizontal OSC frequency is changed by controlling voltage at pin 8.

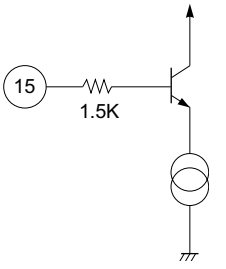



**Fig. 8-19**

(16) Pin 16 is horizontal output terminal.

The output voltage is approx. 5V when the terminal is set in high impedance. And output current becomes approx. 2 mA when the terminal is connected to ground through 100 ohm.

Internal transistor can accept current of approx. 10 mA.

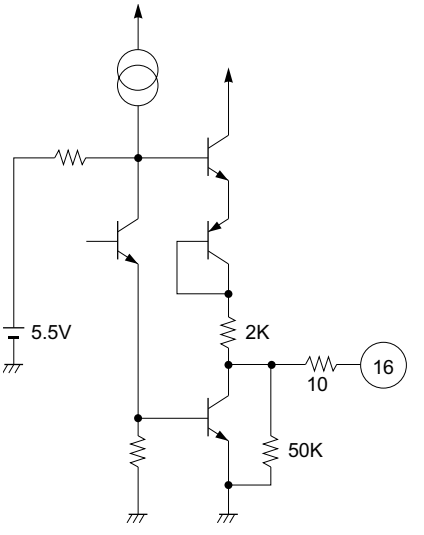



**Fig. 8-20**

(17) Pin 17 is vacant terminal.

(18) Pin 18 is input terminal of FBP

Threshold voltage inside IC is approx. 1.5V. When this voltage becomes 1.5V or more, Mono-multi which is connected to pin 20, begins operation.

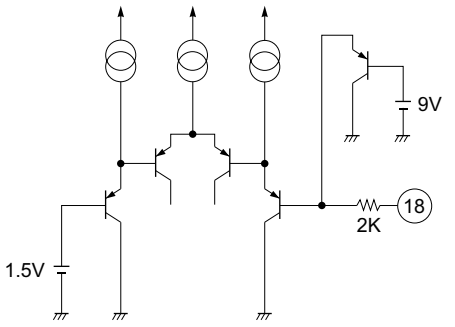



**Fig. 8-21**

(19) Pin 19 is H. LOCK output terminal.

This model does not use this terminal. This terminal gives output of discriminating result of approx. 5V, when horizontal sync signal input from outside of IC and horizontal output at pin 16 are in synchronization.

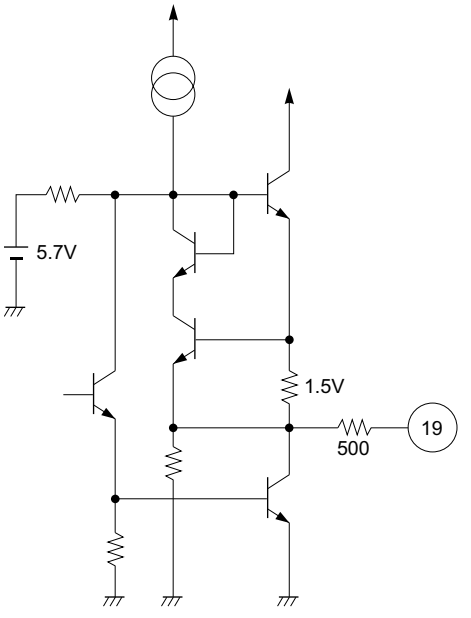



**Fig. 3-22**

(20) Pin 20

FBP which is input from pin 18, is delayed by the time constant of this pin.

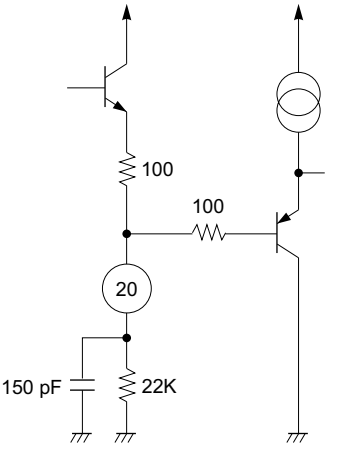



**Fig. 8-23**

(21) Pin 21 is a terminal for power source of the vertical block.

The rated voltage is 12V.

(22) Pin 22

Capacitor for producing AFC comparing wave is connected. The external capacitor is selected so that triangle waveform at pin 22 becomes approx. 2 to 3V.

If wave height is small, the loop-gain of AFC decreases.

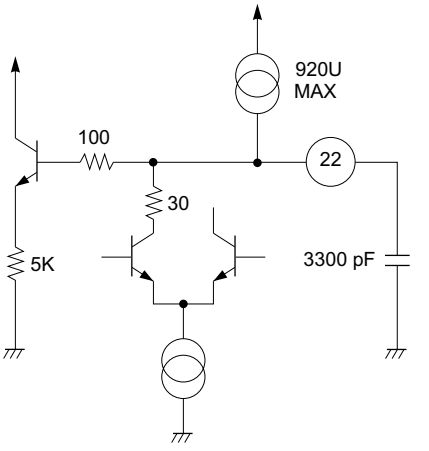



**Fig. 8-24**

(23) Pin 23 is GND terminal of vertical block.

(24) Pin 24 is vertical output terminal.

The output voltage is approx. 5V when the terminal is set in high impedance. And output current becomes approx. 2 mA. When the terminal is connected to ground through 100 ohm.

Internal transistor can accept current of approx. 10mA.

HIGH period of output is 300 ms, and it is independent of frequency of vertical sync signal which is input at pin 30.

By the control voltage of pin 26; V SHIFT terminal, the rising of this pin voltage can be delayed by approx. 0 to 470 ms against the front edge of vertical sync signal.

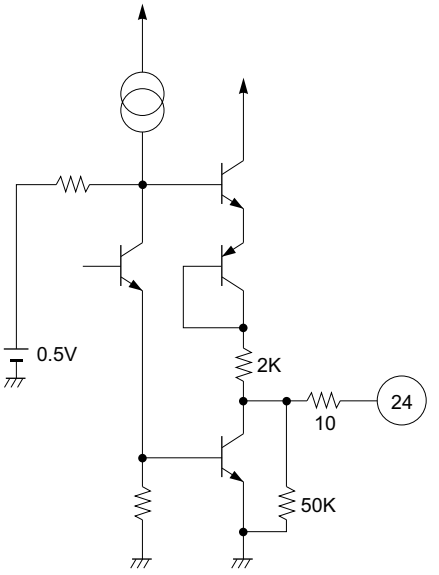



**Fig. 8-25**

(25) Pin 25 is a terminal for vertical blanking output.

The output voltage is approx. 5V when the terminal is set in high impedance.

HIGH period of output is independent of frequency of vertical sync signal which is input at pin 30.

This terminal rises at front edge of vertical sync signal, and the rising is delayed by approx. 100 ms from the rising of pin 24.

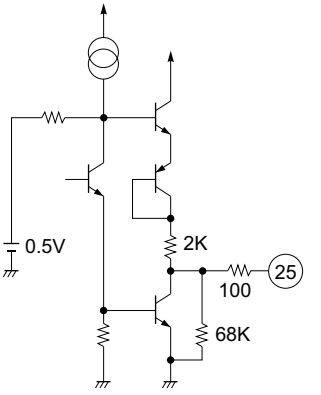



**Fig. 8-26**

(26) Pin 26 is V SHIFT terminal.

The control voltage range is 0 to 2.5V.

When this terminal voltage is 0V, vertical output of pin 24 rises at the same time as vertical sync signal.

By controlling this terminal voltage up to 2.5V, vertical output of pin 24 can be delayed up to 470 ms from the front edge of vertical sync signal.

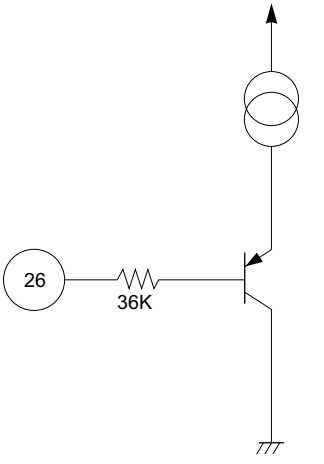



**Fig. 8-27**

(27) Pin 27 is a terminal which is connected with capacitor which produces RAMP waveform output at pins 25 and 26.

Recommended value is 0.015 ㎌, and if this value of capacitor is increased, respective absolute or maximum values of Tvshift, Tvd (pin 24 output), and Tvd-vblk (pin 25 output) can be enlarged, keeping the conditions below.

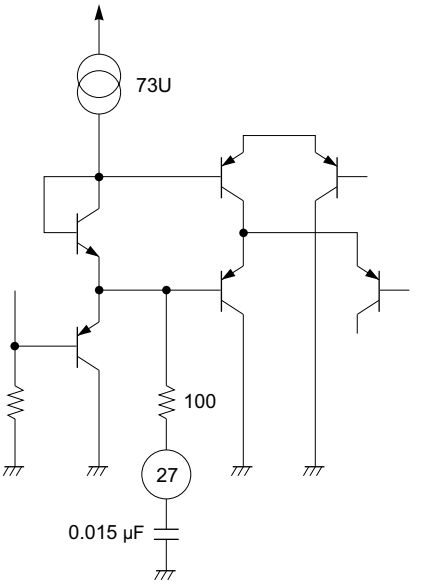
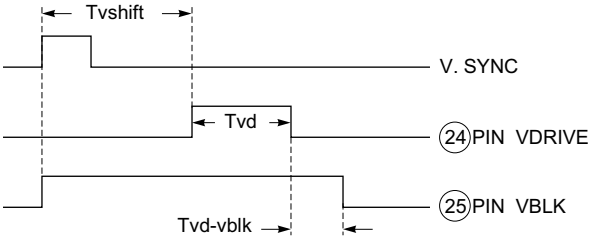



**Fig. 8-28**




Tshift:Tvd:Tvd-vblk=470:300:100

**Fig. 8-29**

(28) Pin 28 is a terminal which produces reference current of vertical OSC circuit and RAMP wave making circuit. The recommended value is 330k ohm.

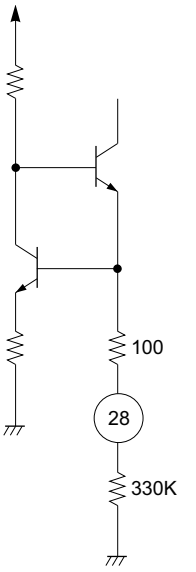



**Fig. 8-30**

(29) Pin 29 is a terminal to connect vertical OSC capacitor.

Using recommended 0.1 ㎌ ±10% allows vertical sync signal ranging from approx. 50 to 160 Hz to be pulled-in with no adjustment.

To shift the pull-in range upper or lower, the value of this capacitor is selected to suitable value. Supposing this capacitor is increased, the pull-in range shifts to lower in both upper and lower limits of frequencies.

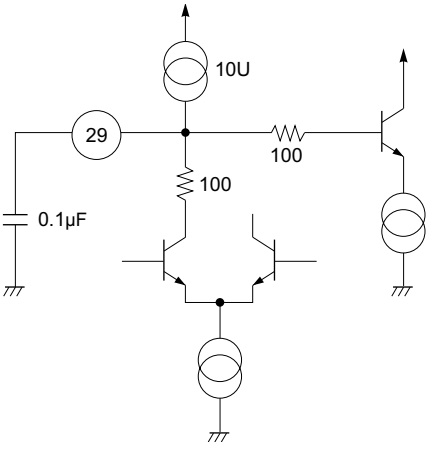



**Fig. 8-31**

(30) Pin 30 is an input terminal of vertical sync signal.

Vertical sync signal of approx. 2 V(p-p) is applied through coupling capacitor 1 mF.

For input sync signal, both polarities of positive and negative can be acceptable, and the sync is triggered at front edge of sync signal.

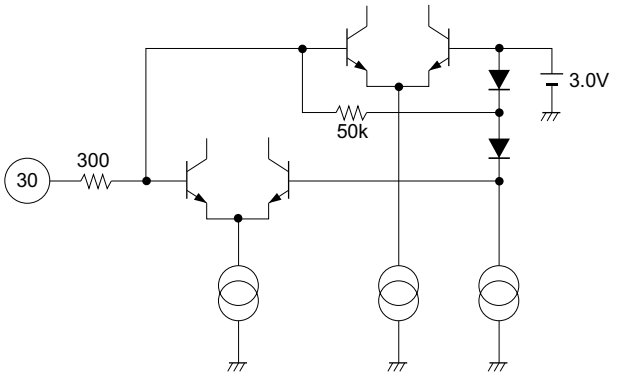



**Fig. 8-32**

## 2-2. Horizontal Phase Shift Circuit

The function to change the horizontal sync signal phase is also provided for the up-converter circuit. However, in fact, the function is not used in manufacturing adjustment with the phase change data determined in designing entered.

When performing the phase adjustment (screen position) in manufacturing, the phase shift circuit built-in LA7860 is used. As previously stated, the DC voltage added to pin 3 can control its phase. The DC voltage is supplied from a D/A converter built-in E/W IC (TA1241).

The main components of this circuit are shown in Fig. 8-33. The output voltage of D/A converter is controlled by the channel selection microprocessor through $I^2C$ bus line. The horizontal phase (screen position) adjustment is carried out by using a remote controller in manufacturing.

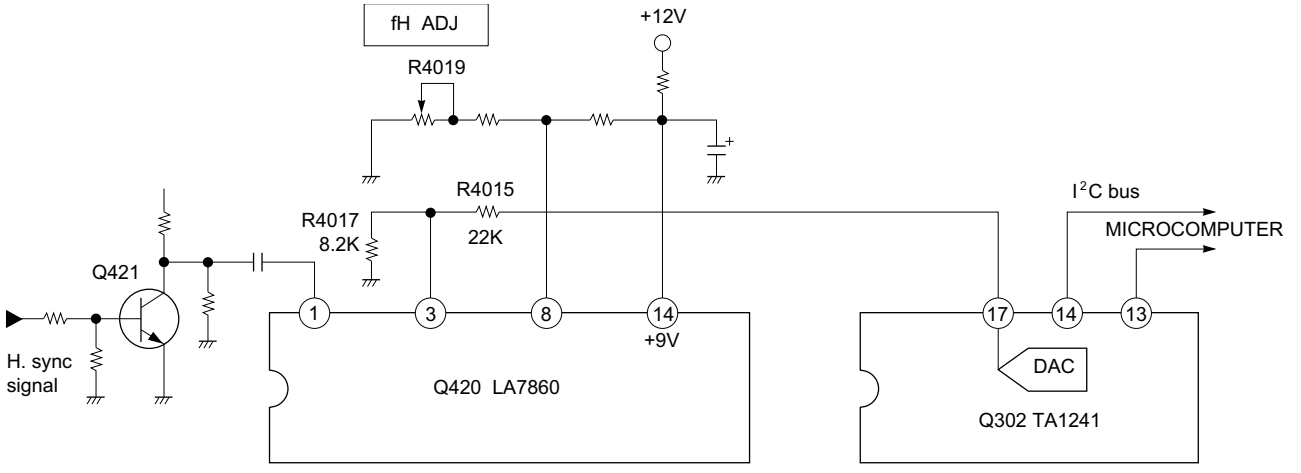



**Fig 8-33 Horizontal phase shift circuit**

# SECTION IX
# VERTICAL OUTPUT CIRCUIT

# 1. OUTLINE

The vertical output circuit of this model has the same components as that of usual PJTV except for a kind of E/W IC (Q302: TA1241). As can be seen from the block diagram, the sync circuit and the vertical oscillation circuit are contained in Q420 (LA7860), and the sawtooth generation circuit and amplifier (vertical drive circuit) contained in Q302 (TA1241). The output circuit and pump-up circuit are included in Q301 (LA7833).

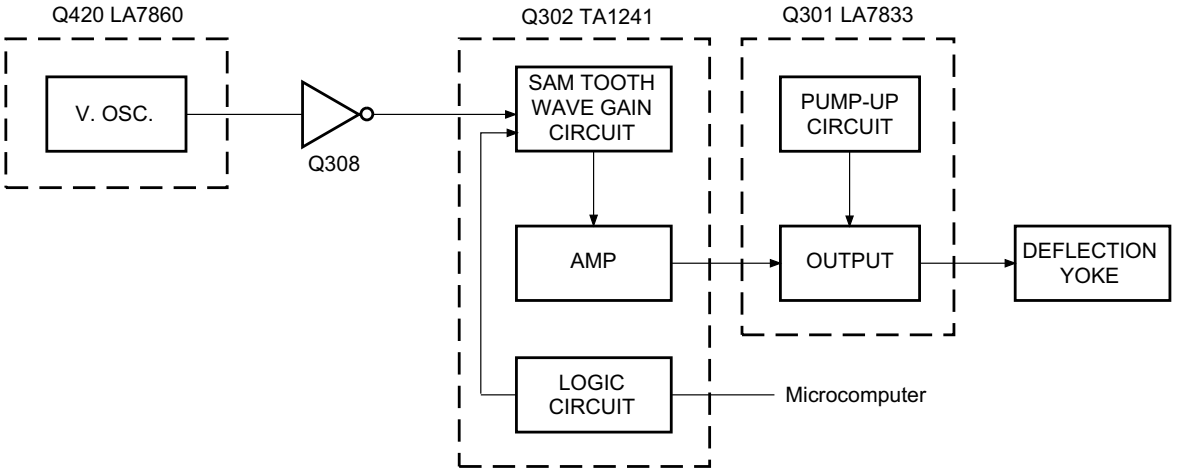



**Fig. 9-1 Vertical deflection circuit block diagram**

## 1-1. Theory of Operation

The purpose of the vertical output circuit is to provide a sawtooth wave signal with good linearity in vertical period to the deflection yoke.

When a switch S is opened, an electric charge charged up to a reference voltage VP discharges in an constant current rate, and a reference sawtooth voltage generates at point (a).

This voltage is applied to (+) input (non-inverted input) of an differential amplifier, A. As the amplification factor of A is sufficiently high, a deflection current flows so that the voltage V2 at point (c) becomes equal to the voltage at point (a).

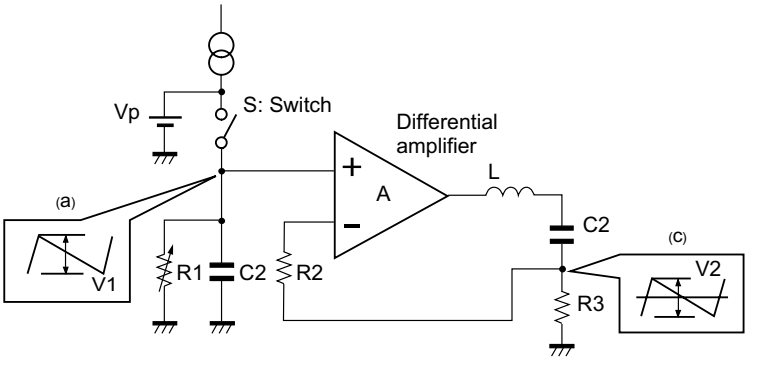



**Fig. 9-2**

# 2. V OUTPUT CIRCUIT

## 2-1. Actual Circuit

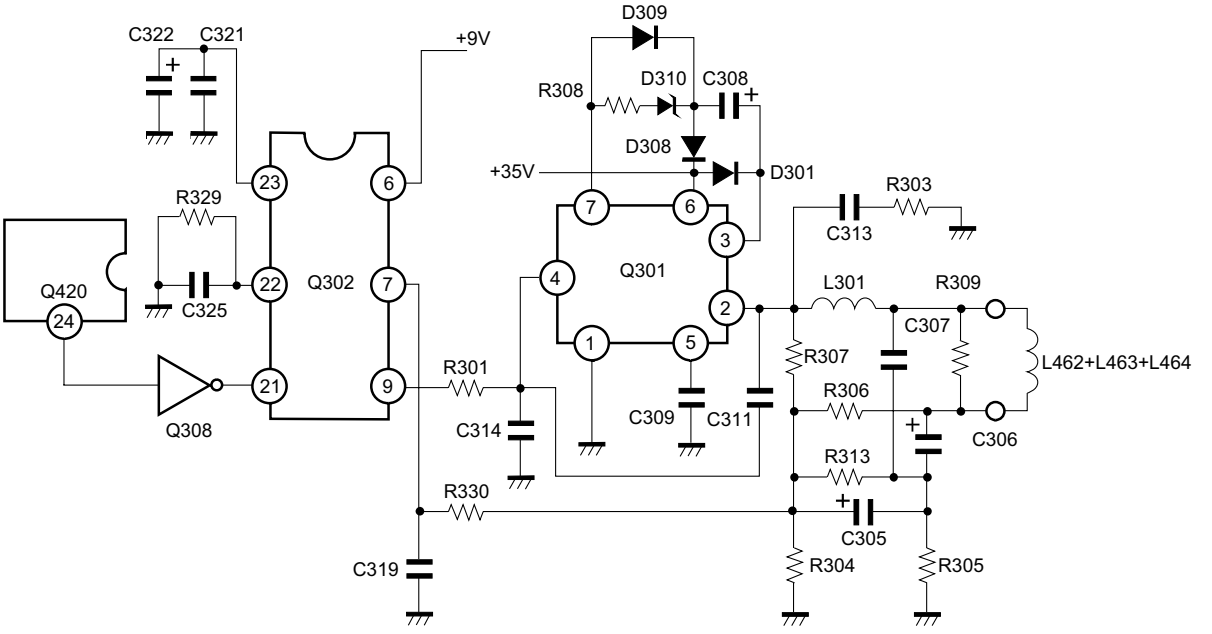



**Fig. 9-3**

## 2-2. Sawtooth Waveform Generation

### 2-2-1. Circuit Operation

The sawtooth waveform generation circuit consists of as shown in Fig. 9-4. When a trigger pulse enters pin 21, it is differentiated in the waveform shape circuit and only the falling part is detected by the trigger detection circuit, to the waveform generation circuit is not susceptible to variations of input pulse width.

The pulse generation circuit also works to fix the vertical ramp voltage at a reference voltage when the trigger pulse enters, so it can prevent the sawtooth wave start voltage from variations by horizontal components, thus improving interlacing characteristics.

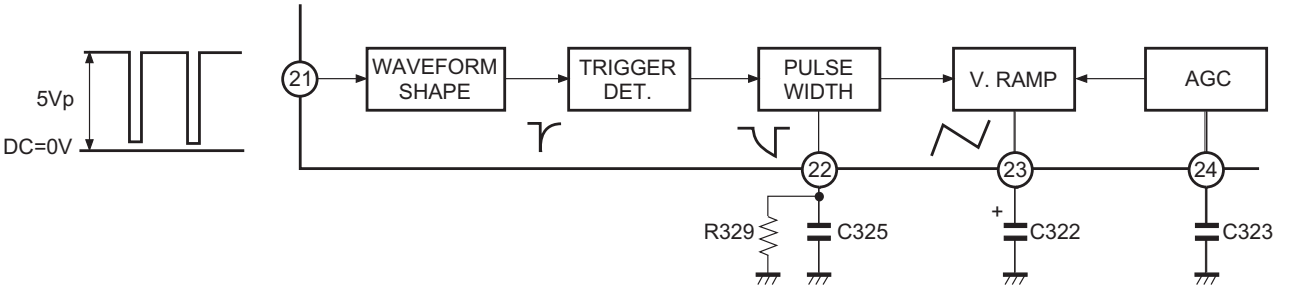



**Fig. 9-4**

## 2-3. Vertical Output

### 2-3-1. Circuit Operation

The vertical output circuit consists of a vertical driver circuit Q302, Pump-up circuit and output circuit Q301, and external circuit components.

(1) Q2 amplifies its input fed from pin 4 of Q301, Q3, Q4 output stage connected in a SEPP amplifies the current and supplies a sawtooth waveform current to a deflection yoke.

Q3 turns on for first half of the scanning period and allows a positive current to flow into the deflection yoke (Q3 ® DY ® C306 ® R305 ® GND), and Q4 turns on for last half of the scanning period and allows a negative current to flow into the deflection yoke (R305 ® C306 ® DY ® Q4). These operations are shown in Fig. 9-5.

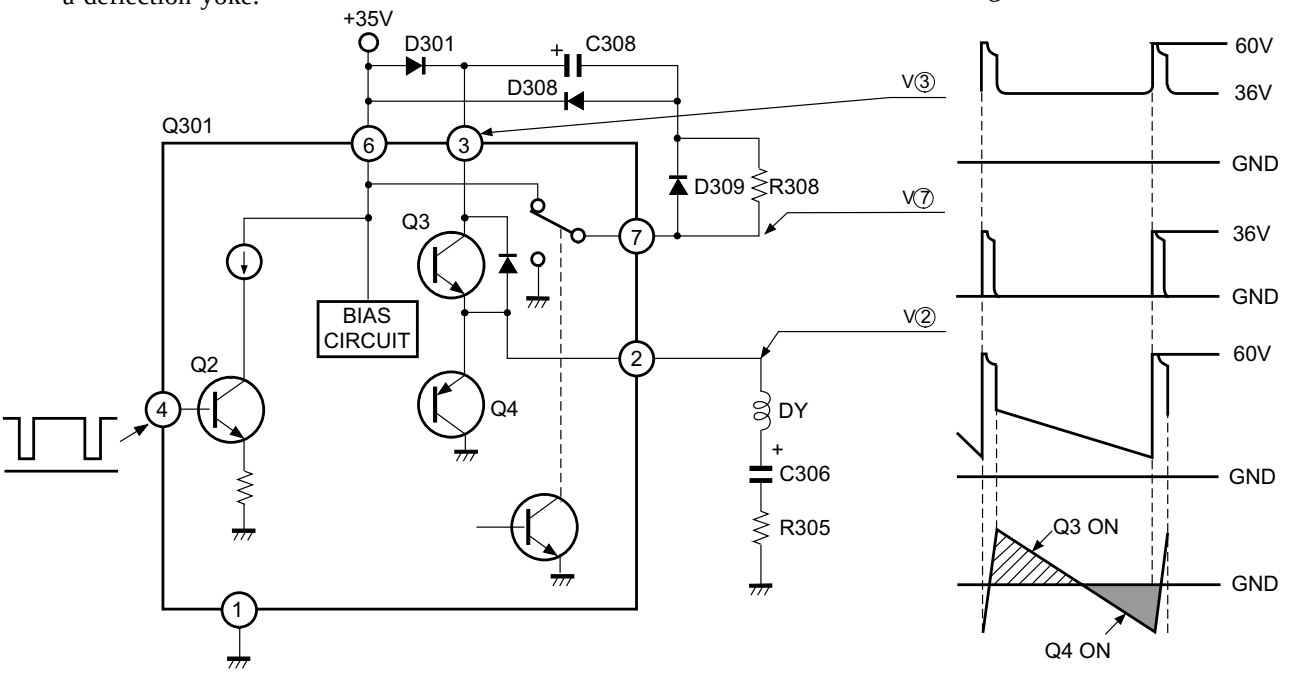



**Fig. 9-5 Vertical output circuit**

(2) In Fig. 9-6 (a), the power Vcc is expressed as a fixed level, and the positive and negative current flowing into the deflection yoke is a current (d) = current (b) + (c) in Fig. 9-6, and the emitter voltage of Q3 and Q4 is expressed as (e).

(3) Q3 collector loss is i1 x Vce1 and the value is equal to multiplication of Fig. 9-6 (b) and slanted section of Fig. 9-6 (e), and Q4 collector loss is equal to multiplication of Fig. 9-6 (c) and dotted section of Fig. 9-6 (e).

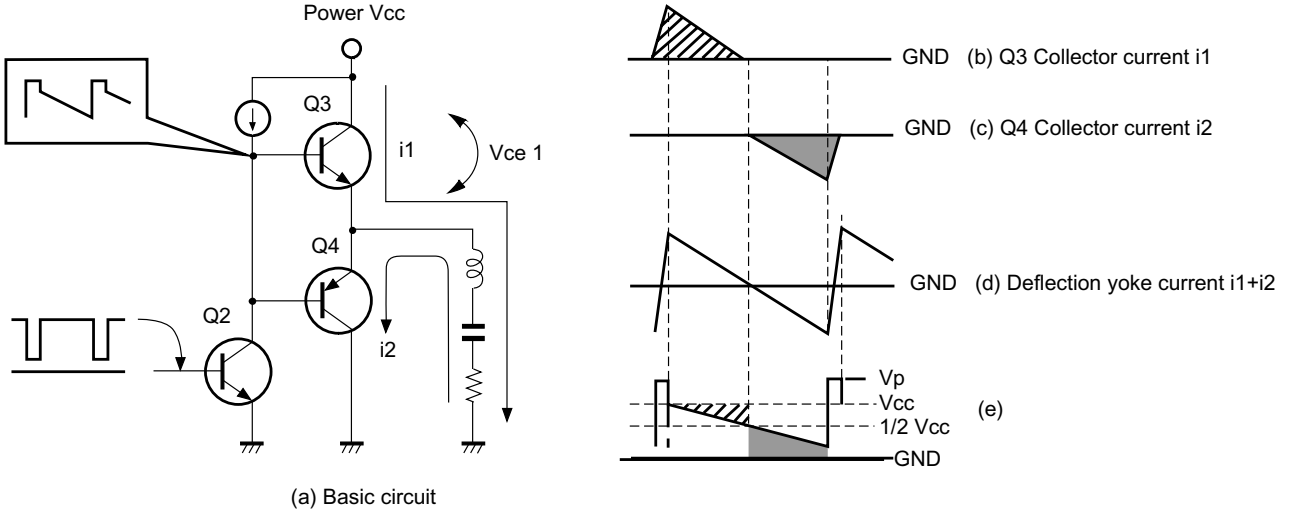



**Fig. 9-6 Output stage operation waveform**

(4) To decrease the collector loss of Q3, the power supply voltage is decreased during scanning period as shown in Fig. 9-7, and $V_{CE1}$ decreases and the collector loss of Q3 also decreases.

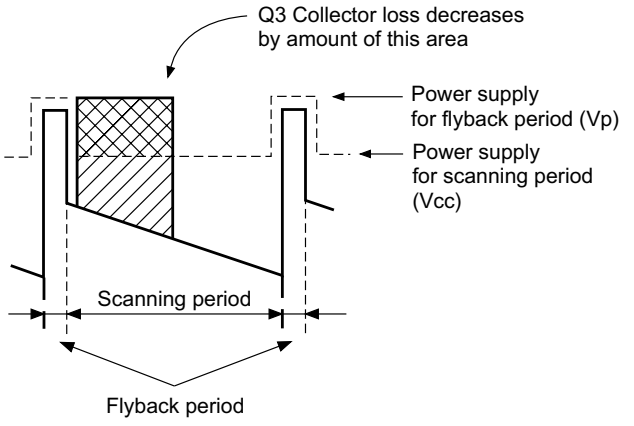



**Fig. 9-7 Output stage power supply voltage**

(5) In this way, the circuit which switches power supply circuit during scanning period and flyback period is called a pump-up circuit.

The purpose of the pump-up circuit is to return the deflection yoke current rapidly for a short period (within the flyback period) by applying a high voltage for the flyback period. The basic operation is shown in Fig. 9-8.

(6) Since pin 7 of a transistor switch inside Q301 is connected to the ground for the scanning period, the power supply (pin 3) of the output stage shows a voltage of ($V_{CC} - V_F$), and C308 is charged up to a voltage of ($V_{CC} - V_F - V_Z - V_R$) for this period.

(7) First half of flyback period

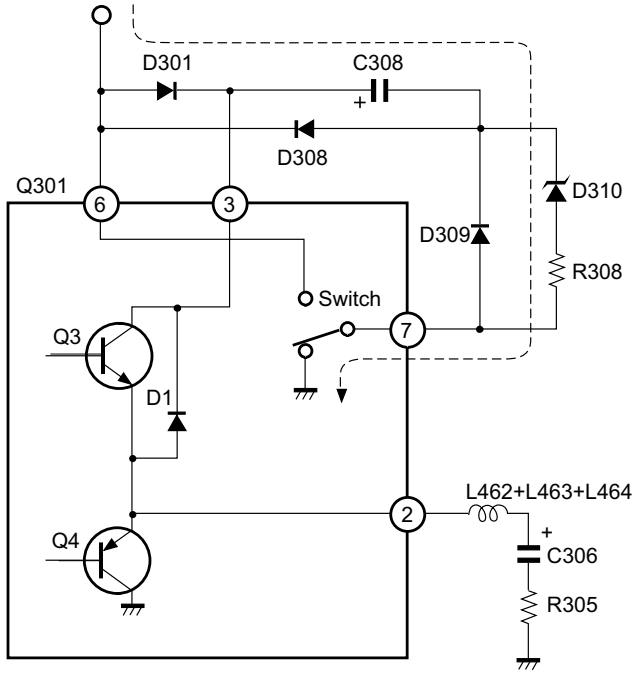
Current flows into L462 → D1 → C308 → D308 → $V_{CC}$ (+35V) → GND → R305 → C306 → L462 + L463 + L464 in this order, and the voltage across these is:

$V_P = V_{CC} + V_F + (V_{CC} - V_F - V_R) + V_F$ about 60V is applied to pin 2. In this case, D301 is cut off.

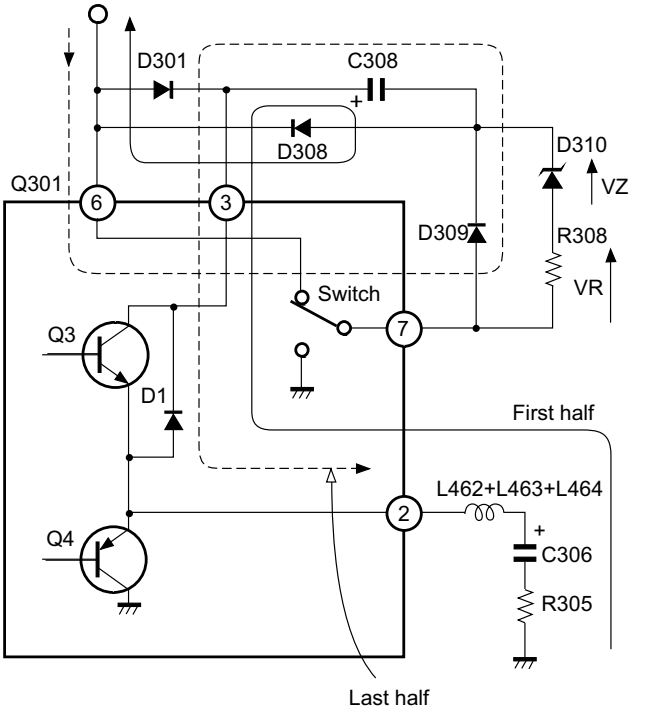
(8) Last half of flyback period

Current flows into $V_{CC}$ ® switch D309 → C308 → Q301 (pin 3) → Q3 → L462 + L463 + L464 → C306 → R305 in this order, and a voltage of $V_P = V_{CC} - V_{CE}$ (sat) $- V_F + (V_{CC} - V_F - V_R) - V_{CE}$ (sat), about 54V is applied to pin 2.

(9) In this way, a power supply voltage of about 36V is applied to the output stage for the scanning period and about 60V for flyback period.




(a) Scanning period




(b) Flyback period

**Fig. 9-8**

## 2-4. Vertical Linearity Characteristic Correction

### 2-4-1. S-character Correction

A parabola component developed across C306 is integrated by R306 and C305, and the voltage is applied to pin 7 of Q302 to perform S-character correction.

### 2-4-2. Up-and Downward Linearity Balance

A voltage developed at pin 2 of Q301 is divided with resistors R307 and R303, and the voltage is applied to pin 7 of Q301 to improve the linearity balance characteristic.

Moreover, the S-character correction and up & downward balance correction are performed through the bus control.

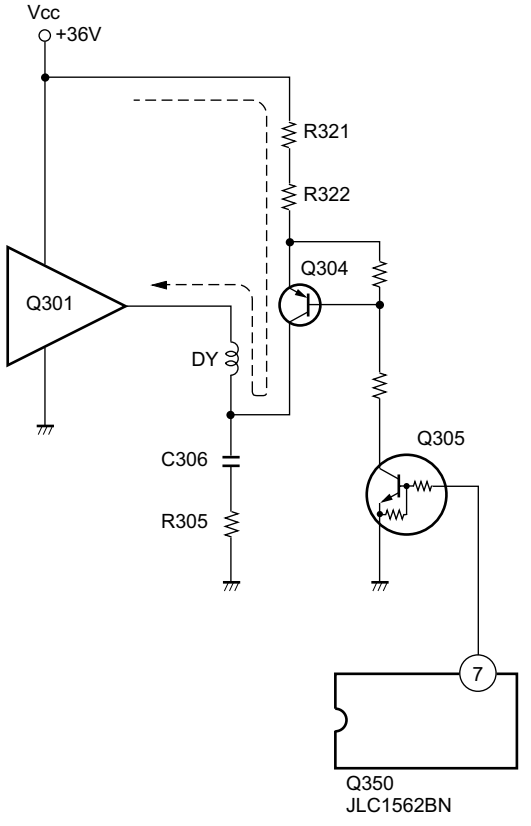



**Fig. 9-9**

## 2-5. Centering Circuit

The centering circuit shown in Fig. 9-9 is only used for the wide model. In the zoom mode of the wide model, the function to move the screen position up and down so as not to hide the characters is required, when the closed caption signal is received.

To move the screen position, as described in the horizontal oscillation circuit, it is necessary to delay the phase of the vertical sync signal by using the up-converter function.

However, to lower the screen position, it is impossible to proceed the phase of sync signal. To solve the problem, after turning on Q305 and Q304, lower the whole raster at first by flowing the DC current to $V_{CC}$ → R321•R322 → Q304 → DY → Q301.

From this status, the screen position is moved up and down by varying the sync signal delay amount.

The voltage to control Q305 and Q304 on/off is supplied from pin 7 of Q350 (I/O expander). The voltage at pin 7 is switched to either high or low through $I^2C$ bus line by the the channel selection microcomputer. In the zoom mode, the voltage at pin 7 develops high level, and Q304 and Q305 turn on.

# 3. PROTECTION CIRCUIT FOR VERTICAL DEFLECTION STOP

When the deflection current is not supplied to the deflection coils, one horizontal line appears on the screen. If this condition is not continued for a long time, no trouble will occur in a conventional TV. But in the projection TV, all the electron beams are directly concentrated at the fluorescent screen because of no shadow mask used, and burns out the screen instantly.

To prevent this, the stop of the vertical deflection is detected when the horizontal one line occurs, and the video signals are blanked out so that the electron beams are not emitted.

When the vertical deflection circuit is operating normally, a sawtooth wave voltage is obtained across (R305), so Q384 repeats on-off operation in cycle of vertical sync.

In this case, the collector voltage of Q385 is set to (12V – $V_{CEsat}$ (Q385)) with R386 and C388 as shown in Fig. 9-10. Accordingly, Q385 and Q386 are continuously turned on. As a result, diode D382 is turned off, giving no influence on the blanking operation.

Next, when the vertical deflection stops, the voltage across (R305) does not develop, so Q384 turns off, and both the Q385 and Q386 are turned off. Then, the picture blanking terminal pin 25 of Q501 is set to high through R387 and D382 connected to 12V power line, BLANKING CIRCUIT ON thus cutting off the projection tubes.

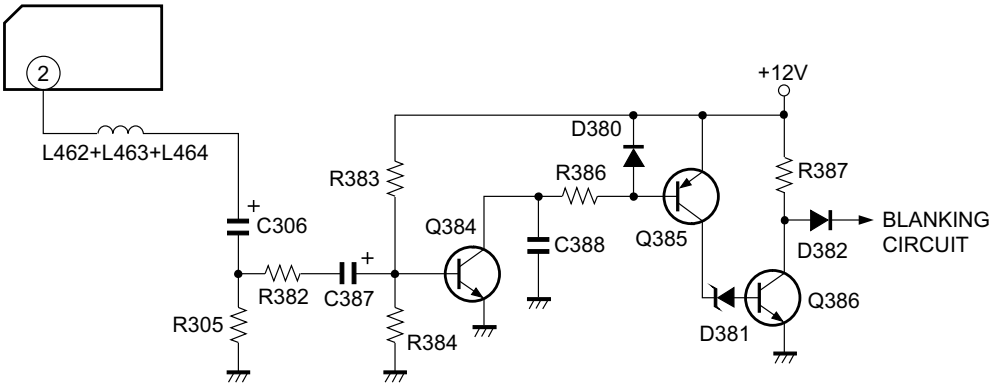



**Fig. 9-10**

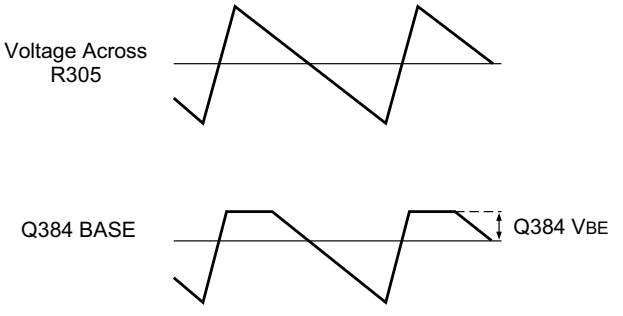



**Fig. 9-11**

## 3-1. +35V Over Current Protection Circuit

The over current protection circuit cuts off the power supply relay when it detects abnormal current increased in the +35V power line due to failure of the vertical deflection circuit.

### 3-1-1. Theory of Operation

Fig. 9-12 shows the circuit diagram of the over current protection circuit. When the load current of the +35V line increases, the voltage across a resistor of R370 will also increase. When the voltage increases across R370 and the voltage developed across R371 becomes higher than the $V_{BE}$ of Q370, Q370 turns on and a voltage develops across R374 due to the collector current flowing. When this voltage increases to a value higher than about 1.3V, SCR•D846 operates, thus cutting off the power relay. When the circuit operates, a power LED provided will turn on and off in red.

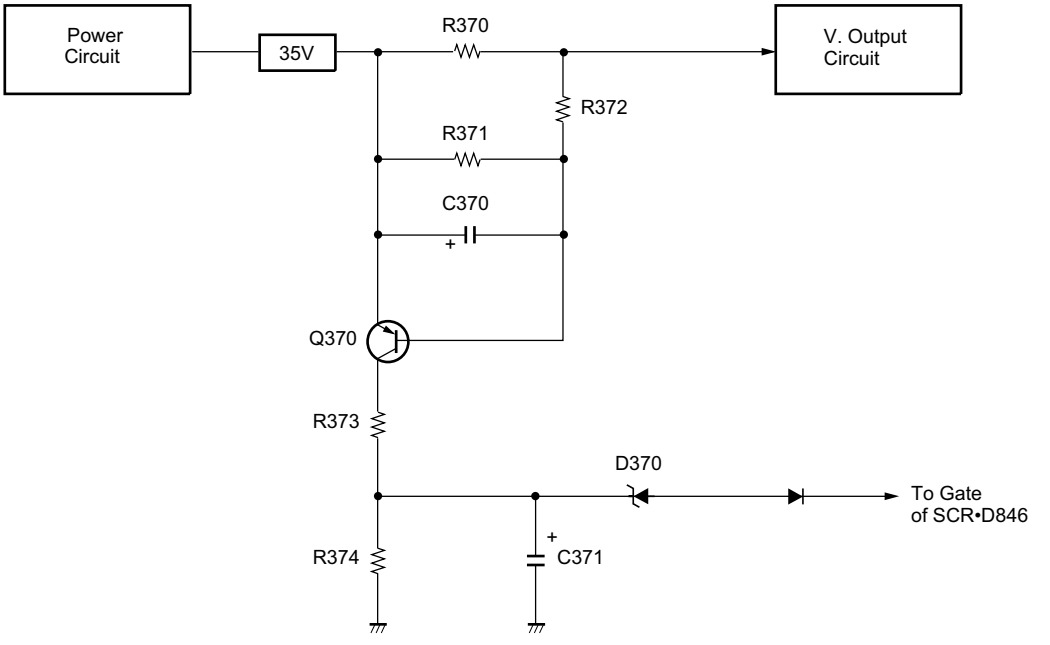



**Fig. 9-12**

# SECTION X
# HORIZONTAL DEFLECTION CIRCUIT

# 1. OUTLINE

A normal PJTV uses one circuit which realizes two functions: one flows a deflection current in the deflection yoke and the second applies a high voltage to the anode of CRT. However, in this model, these two functions are separated and realized in two circuits, so that the high voltage regulation is improved to apply high voltage to CRT to improved the focus as well as improving the size regulation. Hereinafter, the former is called DEFLECTION CIRCUIT, and the latter HIGH VOLTAGE CIRCUIT. The basic operation principle of these circuits is the same as a normal TV circuit. HIGH VOLTAGE CIRCUIT is explained first.

# 2. HIGH VOLTAGE CIRCUIT

Fig. 10-1 shows the block diagram.

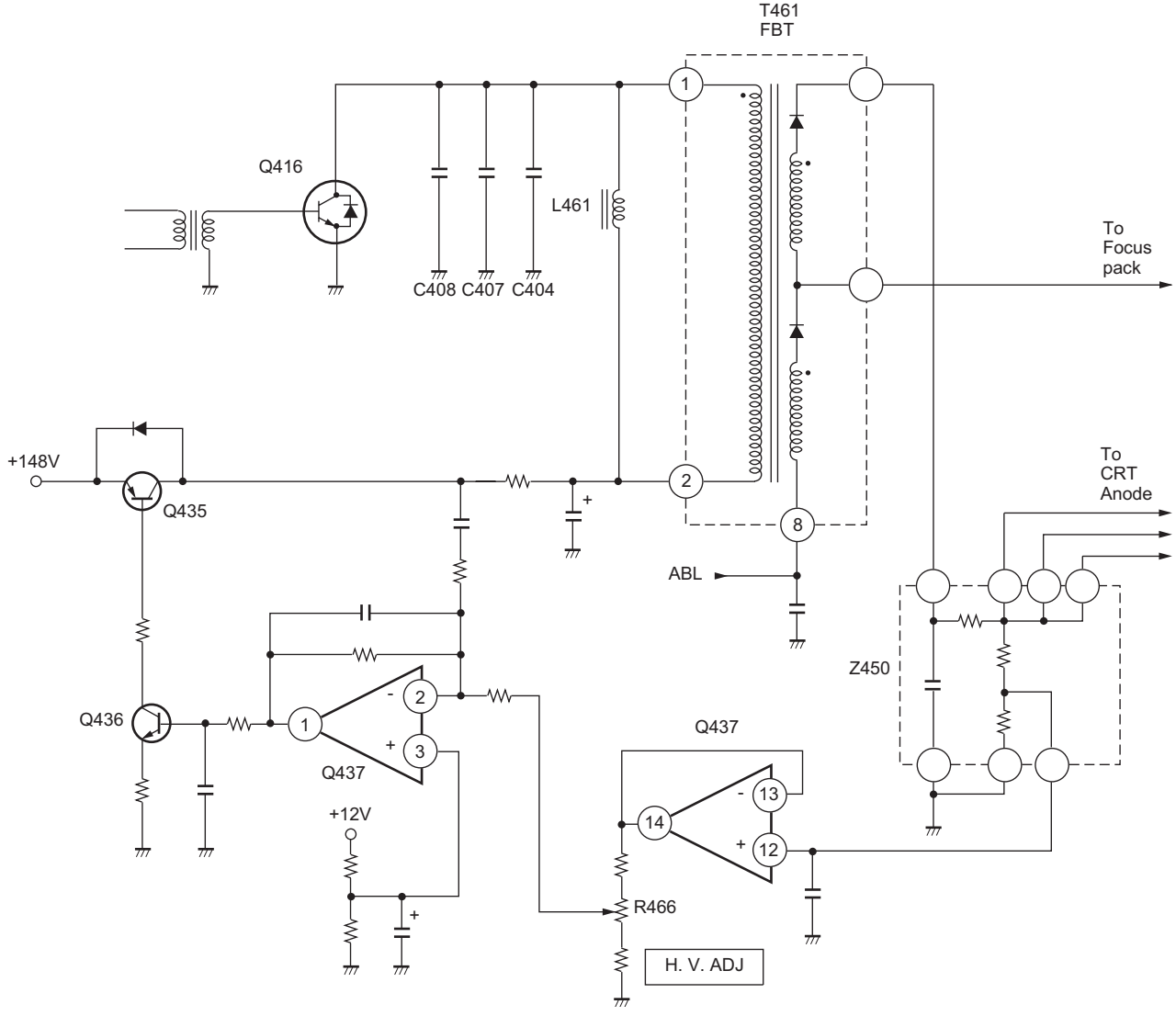



**Fig. 10-1 Block Diagram of HIGH VOLTAGE CIRCUIT**

## 2-1. General

L461 is a choke coil which corresponds to an deflection yoke in a normal TV. A flyback pulse is generated in the primary side of FBT and it is booted with a transformer. This operation is entirely the same as that of a normal TV circuit. So the explanation of this operation is omitted. Only the difference is that the voltage to be applied to pin 2 of FBT is controlled with the series regulator of Q435, Q436, Q437. This series regulator is used to form a high voltage regulator. The regulator detects the high voltage output of FBT by dividing it with a resistor, controls the detected voltage (at pin 12 of Q437) to be constant, and holds the high voltage at a constant value (31 kV). Overcontrol may result in an excessive peak power when a white belt appears. So the AC gain of the error amplifier is considerably lowered. Therefore, a slight voltage ripple occurs in the high voltage. Distortion accompanying the ripple is corrected in the DEFLECTION CIRCUIT. Pins 12 to 14 of Q437 operational amplifier work as a buffer amplifier, and pins 1 to 3 as an error amplifier of the regulator.

## 2-2. X-ray Protection Circuit

This circuit prevents dangerous radiation of X-ray from the CRT when the voltage created with FBT is abnormally increased due to a failure in any part. Fig. 10-2 shows the block diagram of this circuit.

If the voltage generated in FBT abnormally increases, a pulse that is generated in other winding of FBT also increases. To prevent this, the pulse that is generated in the winding between pins 4 and 9 is peak rectified, so that the protection circuit works when this voltage increases over a prescribed level. D471 rectifies the pulse, C471 smoothes it, and R451/R452/R453 divide the voltage and apply it to the emitter of Q430. If the emitter voltage increases higher than the value obtained by adding the zener diode of D472 to $V_{BE}$ of Q430, Q430 turns on and Q429 also turns on. When Q429 turns on, a voltage is applied to the gate of SCR/D846 which forms the protection circuit of the power supply circuit and the SCR turns on. When the SCR turns on, the relay of the power supply circuit opens, the AC current is not supplied to the switching power supply and the set stops operation. This state is held until the AC power cord plug is disconnected. When the AC plug is disconnected and the 5V – 1 for the channel selection circuit is sufficiently lowered, the SCR is turned off and restored. In addition, the vertical output circuit, the converter output circuit and the main B line overcurrent protection circuit are connected to the gate of the SCR.

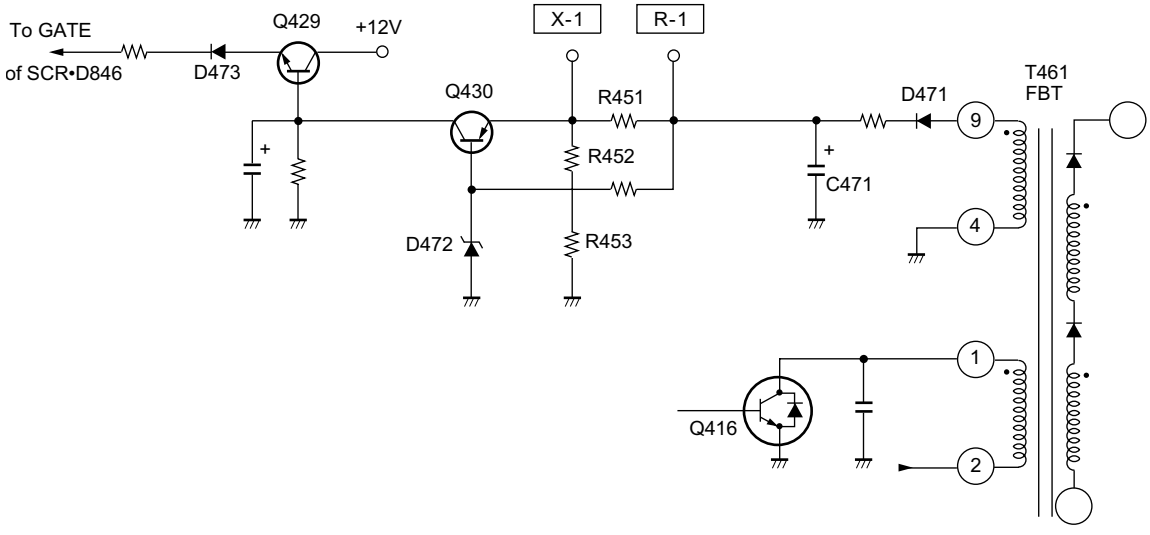



**Fig. 10-2 X-ray protection circuit block diagram**

## 2-3. 200V Low Voltage Protection Circuit

Fig. 10-3 shows a block diagram of this circuit.

The 200V line power taken from the FBT is supplied to the video output circuit of the CRT-D unit. If this voltage decreases, the CRT cathode voltage lowers and an excessive cathode current flows out causing a damage in the CRT. To prevent this, the protection circuit is provided so that when the 200V drops, the set stops operation. As shown in Fig. 10-3, the 200V line voltage is divided with a resistor and is applied to pin 10 of IC (Q302). The pin 10 is internally connected to the comparator's input terminal.

The other input terminal of the comparator is supplied with a reference voltage of 6.25V. If the voltage at the pin 10 drops to lower than 6.25V, it is judged occurrence of any error. The result of this judgment is read with the tuning microcomputer through the $I^2C$ bus. The microcomputer turns off the power and turns on and off the red LED flicker on the front of the set. Unlike when the power supply protection circuit D846 (described above) turns on, the set resumes operation by turning the power on through a remote controller.

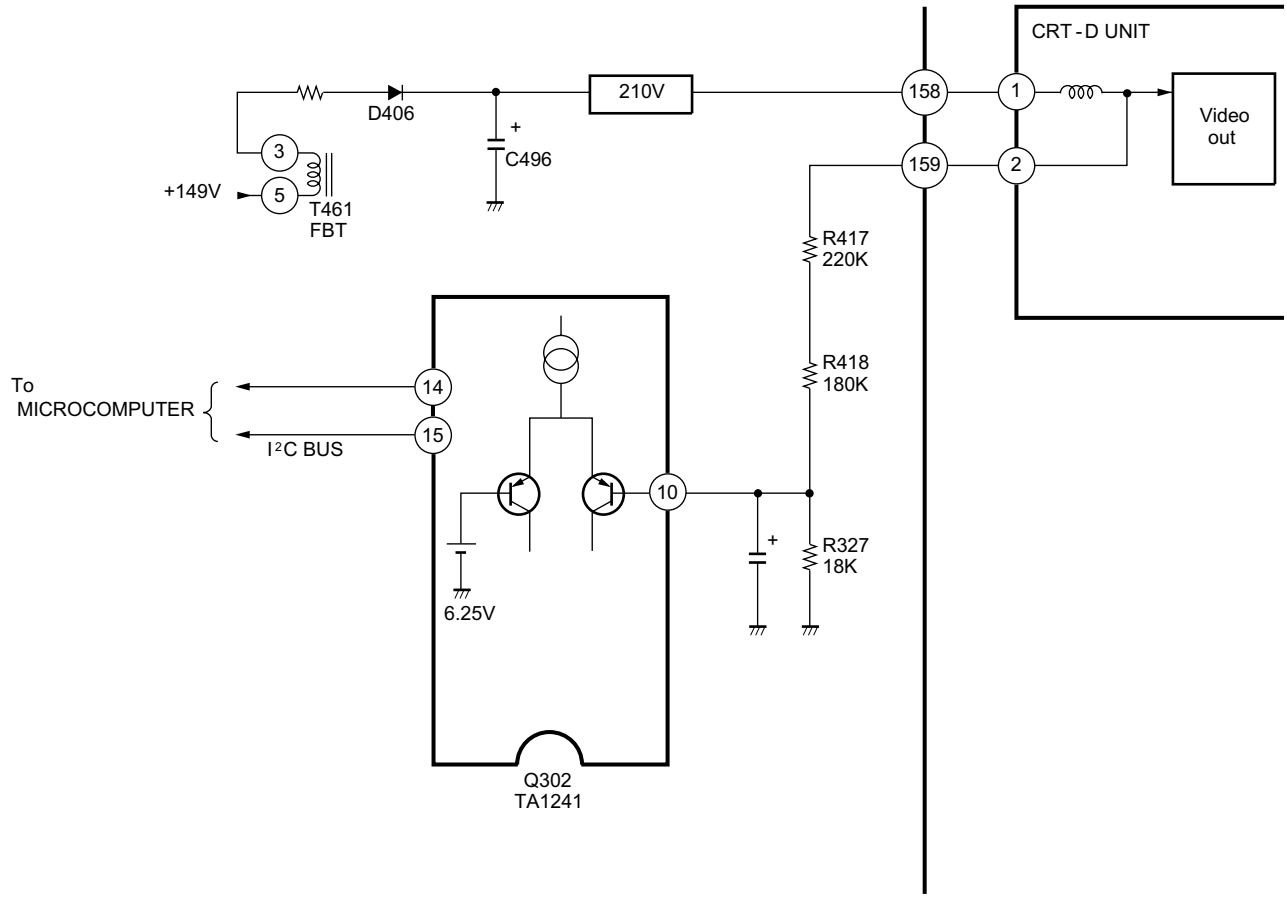



**Fig. 10-3 200V low voltage protection circuit block diagram**

# 3. DEFLECTION CIRCUIT

Fig. 10-4 shows the primary circuits.

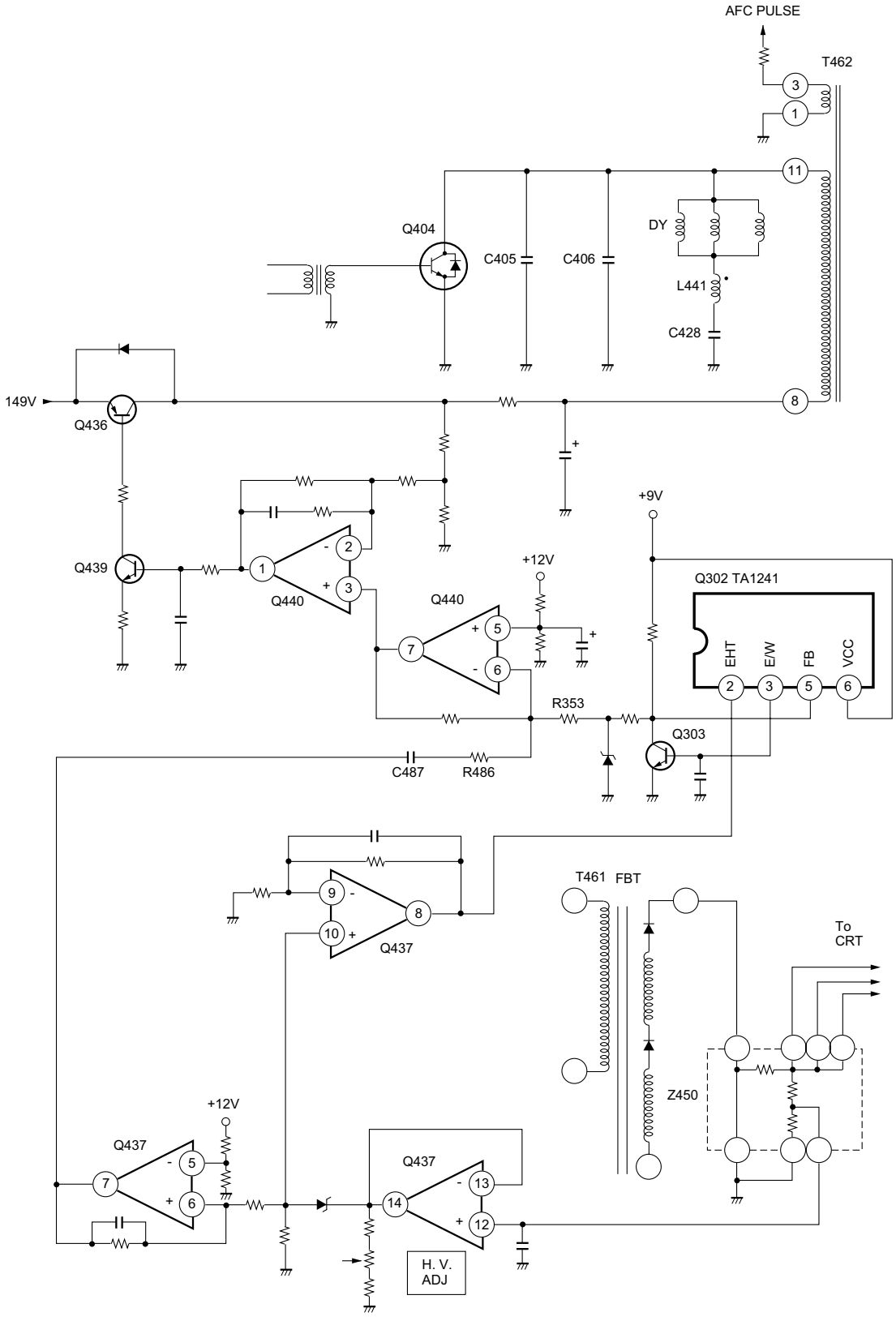



**Fig. 10-4 Deflection circuit diagram**

## 3-1. General

T462 in Fig. 10-4 is a transformer which corresponds to FBT in a normal TV circuit. However, in this model, an AFC pulse is taken from this transformer and is applied to the horizontal oscillation circuit and V/C/D IC. Like the high voltage circuit, the basic operation is the same as that of a normal TV circuit, and the explanation is omitted. Only the difference is that the series regulator is used to control the horizontal width and to correct E/W distortion. This series regulator comprises Q436, Q439 and Q440. The horizontal width and E/W distortion correction voltage is controlled by the voltage at pin 3 of E/W IC Q302 through Q303 and R353. The voltage generated at the pin 3 is controlled with the channel selection microcomputer through the $I^2C$ bus. Therefore, the horizontal width and E/W distortion can be adjusted by using a remote controller, for example. Complete correction of the E/W distortion causes excessive loss in the series regulator. So it is corrected 50%, and another 50% is corrected with the digital convergence. Therefore, for the E/W distortion adjustment data, the value determined when designing is entered and adjustment for each set is not made in the production process. In addition to the horizontal width and E/W distortion control voltage (described above), a voltage to correct distortion such as WPD caused by a high voltage ripple is also applied to the pin 6 of the ope. amplifier Q440. The high voltage ripple waveform is reverse amplified and is supplied from the pin 7 of the ope. amplifier Q437 through R486 and C487. The waveform obtained by amplifying the high voltage ripple is applied also to the EHT terminal (pin 2) of E/W IC Q302. This controls the vertical width and corrects a change in the vertical width caused by the high voltage ripple. The drive circuit uses an FET. The scanning frequency is as high as 31.5 kHz. If the storage time is different, the drive pulse duty ratio largely changes and the horizontal out loss increases. This is the same for the high voltage circuit. A push-pull predrive circuit is provide to drive the FET. The operation principle is the same as a normal PJTV, except the transistor.

## 3-2. S-character Capacitor Switching

As the circularity at the center of the screen is set high in the theater mode of the wide model, the horizontal linearity is set so that the center of the screen shrinks and both ends expand. To realize this horizontal linearity, the switching circuit which increases the S-shaped capacitor capacity is added in the theater mode of the wide model.

Fig. 10-5 shows the block diagram of this switching circuit. When the theater wide mode is selected, Q491 and Q490 turn on and the relay SR41 closes. In addition to C428 and C429 which have been connected, C491 is connected in parallel to increase the capacity. At this time, C411 is connected in parallel to C412. C411 is a capacitor of the dynamic focus circuit. As the S-shaped capacitor increases in capacity, the parabolic voltage generated at both ends becomes small and the dynamic focus voltage amplitude becomes small. With the capacity increased, the voltage applied to the primary winding of the focus transformer is increases to adjust the dynamic focus amplitude. The voltage to turn on Q491 is supplied from the pin 6 of the I/O expander Q350. Q350 is controlled with the tuning microcomputer through the $I^2C$ bus line. Since the horizontal linearity is changed as described above, the final linearity is determined by adjusting the digital convergence though the S-shaped capacitor is switched. In PJTV, regardless of the display mode, the horizontal or vertical linearity is finally determined by adjusting the digital convergence.

## 3-3. Horizontal Stop Protection circuit

As the high voltage circuit continues operation even if the deflection circuit fails and stops, a vertical line remains on the screen burning the CRT fluorescent surface. To prevent this, a protection circuit is provided to stop the whole set when the deflection circuit fails and stops. Fig. 10-6 shows this circuit. The protection circuit detects the AFC pulse of the transformer T462 which corresponds to an FBT. Rectifying the AFC pulse with D451, it generates an DC voltage.

The voltage is approximately 65V when the set is normal. Dividing the voltage with R490 and R492 and applying to Q451, a voltage of about 11.0V can be obtained at the emitter of Q452. Q452 turns on, the voltage at the collector of Q452 drops to 3.5V the same voltage at the emitter, and the zener diodes D454 and D456 turn off. This is the operation flow in a normal state. If any error occurs and the AFC pulse becomes small, Q452 turns off and the voltage at its collector rises to 12V. Then, D454 and D456 turn on and blank the video signal, and at the same time they actuate the protection circuit of the power supply circuit stopping the set. The circuit of Q441, D440 and C450 prevents a malfunction when the above protection circuit turns on the power switch. When the protection circuit turns on the power switch, a charging current flows from C450 to Q441 and Q441 turns on grounding the anode of D454.

Therefore, the power supply protection circuit does not work. The protection circuit explained above is effective also when the winding of pins 3 and 1 of T462 are shorted, preventing T462 from burning. Another protection circuit which has the same configuration as that of Q451 and Q452 is connected to the pin 6 of the transformer T462. This protection circuit comprising Q431 and Q432 detects the pulse that is smaller than the pulse, and the resistance value is different accordingly. This protection circuit also works when the pulse becomes small, but the main purpose is to protect the transformer from burning when the winding of T462 is shorted.

When the windings between the pins 6 and 5 and between the pins 4 and 5 are shorted, this protection circuit works. These windings are not used at all, and an unnecessary winding exists because the existing transformer is used. The transformer burns when the secondary winding is shorted. Because, as the turn number of the secondary winding is small, combining with the primary winding is weak, and influence of the short-circuit does not almost appear in the primary side and the operation continues as normal. This makes a large current flow in the secondary winding. As a result, the secondary winding is heated and burnt.

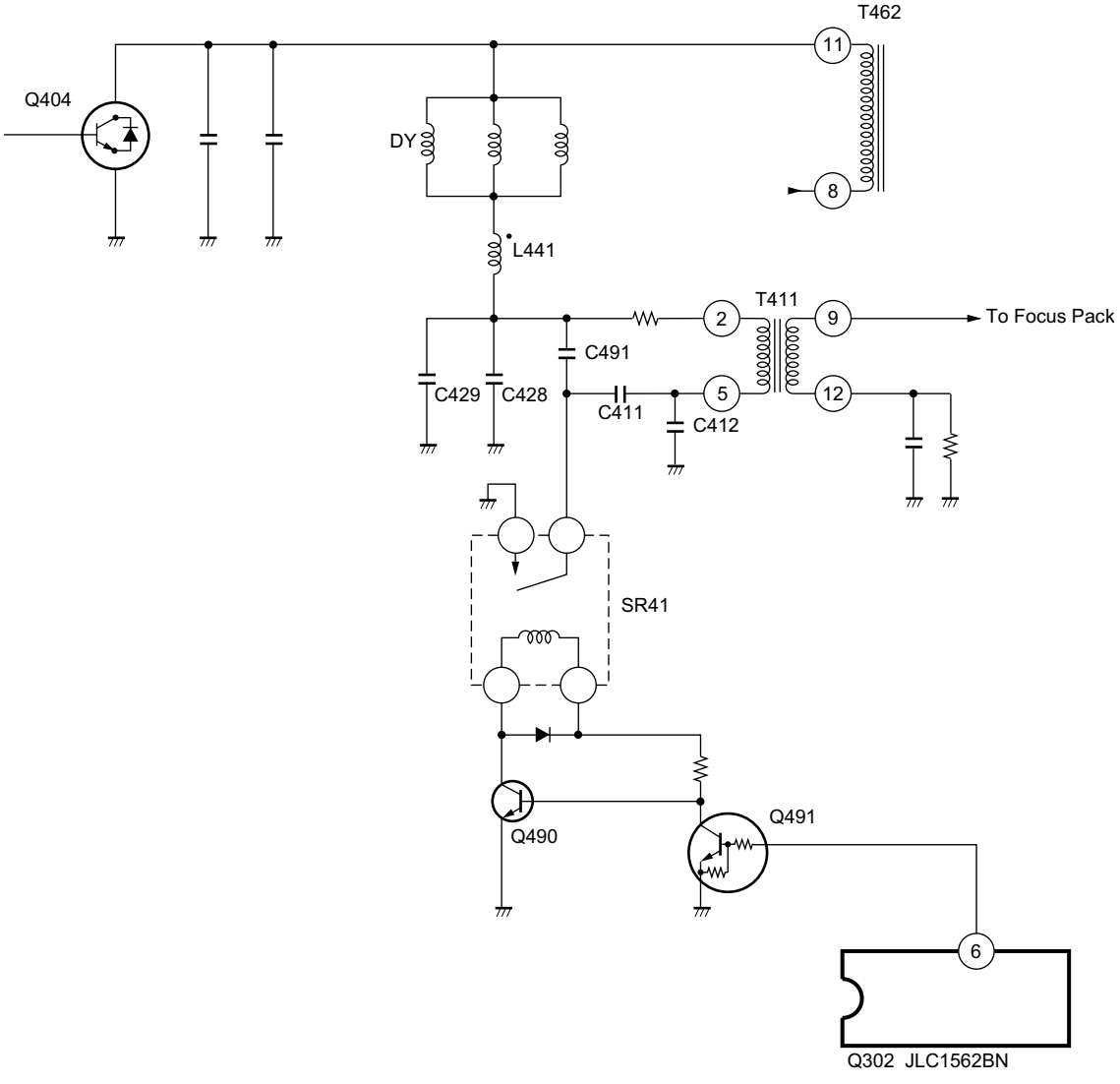



**Fig. 10-5 S character capacitor switching circuit**

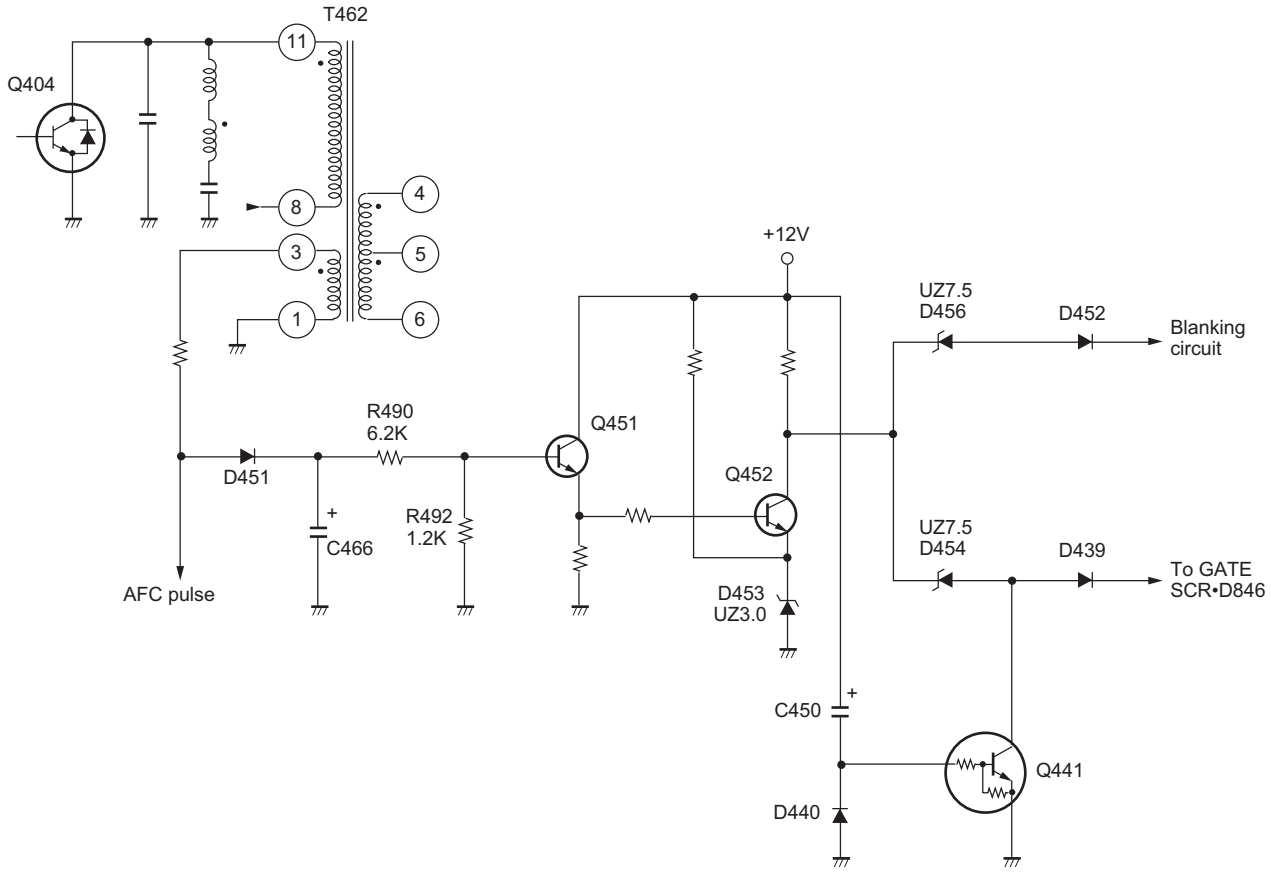



**Fig. 10-6 Protection Circuit diagram**

## 3-4. CRT Protection Circuit

This circuit stops operation of the spot killer circuit to prevent the CRT fluorescent surface from burning when the vertical circuit or deflection circuit fails. The spot killer circuit operation is explained first. If the anode voltage is held high after the power supply is turned off, the CRT surface may bright as a spot because of radiation of electron from dust in the CRT even if no signal is applied to other electrode. To prevent this, a large anode current is made run at the moment when the power is turned off, so that the high voltage applied to the anode electrode is decreased as far as possible. The circuit called a spot killer performs this function.

The spot killer circuit comprises C965 and Q967 in this block diagram. C965 and C966 are charged, so that while the power is being supplied, the voltage at both ends of C966 is Vf. Therefore, Q967 is held off. When the power is turned off, the 9V power supply voltage begins to decrease, and the emitter voltage of Q967 is also decreased by the voltage charged at both ends of C965. When Q967 turns on, a current is taken out from the emitter of the transistor in the upper stage of the video output circuit that is connected in cascade.

As a result, the cathode voltage of CRT suddenly drops, a large cathode current flows, and the high voltage is decreased. Therefore, if an error which cause stop of a deflection current and the protection circuit of the power supply circuit works to stop operation of the set, the spot killer circuit works and the fluorescent surface of the CRT is burnt due to the large cathode current. This occurs often if the 35V overcurrent protection circuit of the vertical output circuit or the horizontal stop protection circuit works. So, when the protection circuit of the power supply circuit works, the spot killer circuit is made ineffective to protect the CRT. The circuit comprising Q483 and Q4 in Fig. 10-7 is the CRT protection circuit. When a trigger is applied to the gate of the SCR D846 used in the protection circuit of the power supply circuit, Q483 also turns on at the same time. Q484 also turns on and runs the current toward C965 of the spot killer circuit to prevent the emitter voltage of Q967 from being dropped and Q967 from being turned on.

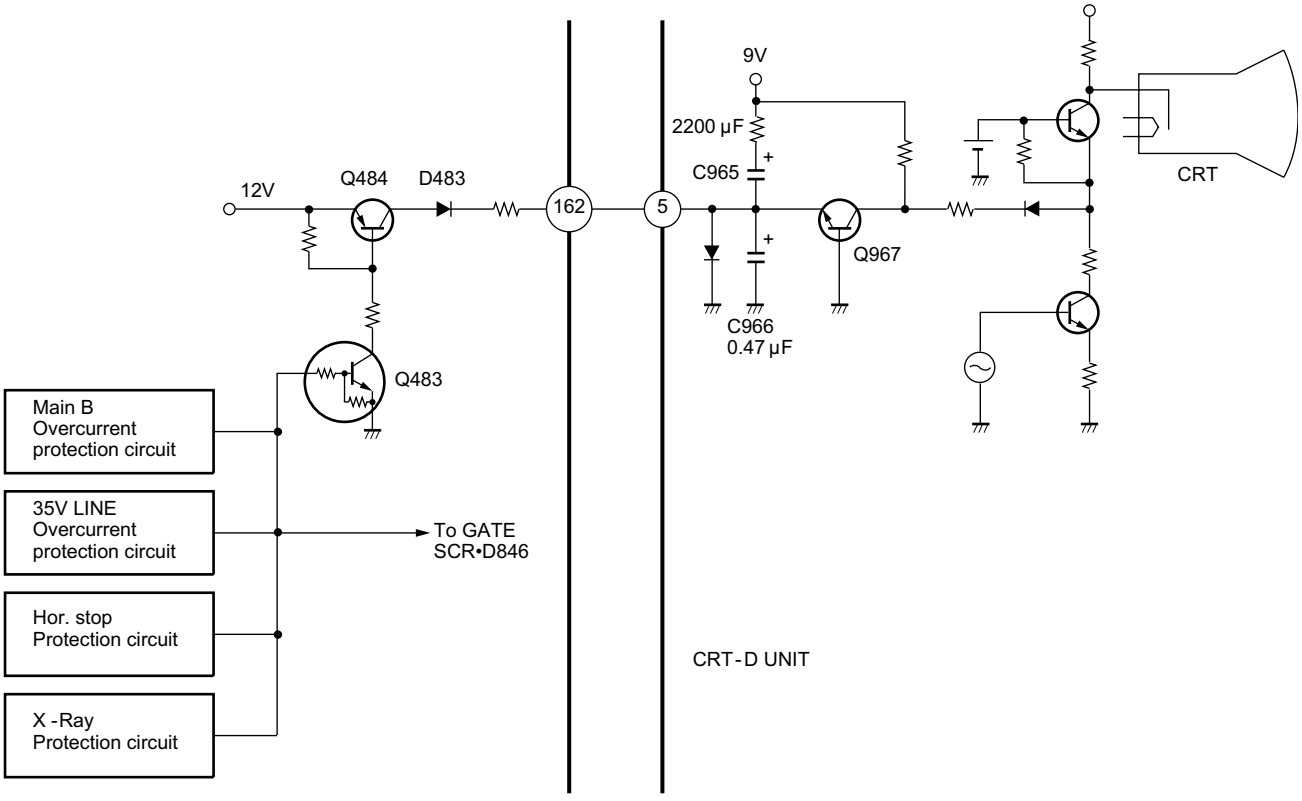



**Fig. 10-7 CRT Protection Circuit**

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# SECTION XI
# DYNAMIC FOCUS CIRCUIT

# 1. OUTLINE

In PJTV, the parabola voltages of the horizontal and vertical sync are superimposed on the focus voltage to improve the focus quality. Fig. 11-1 shows the dynamic focus circuit diagram.

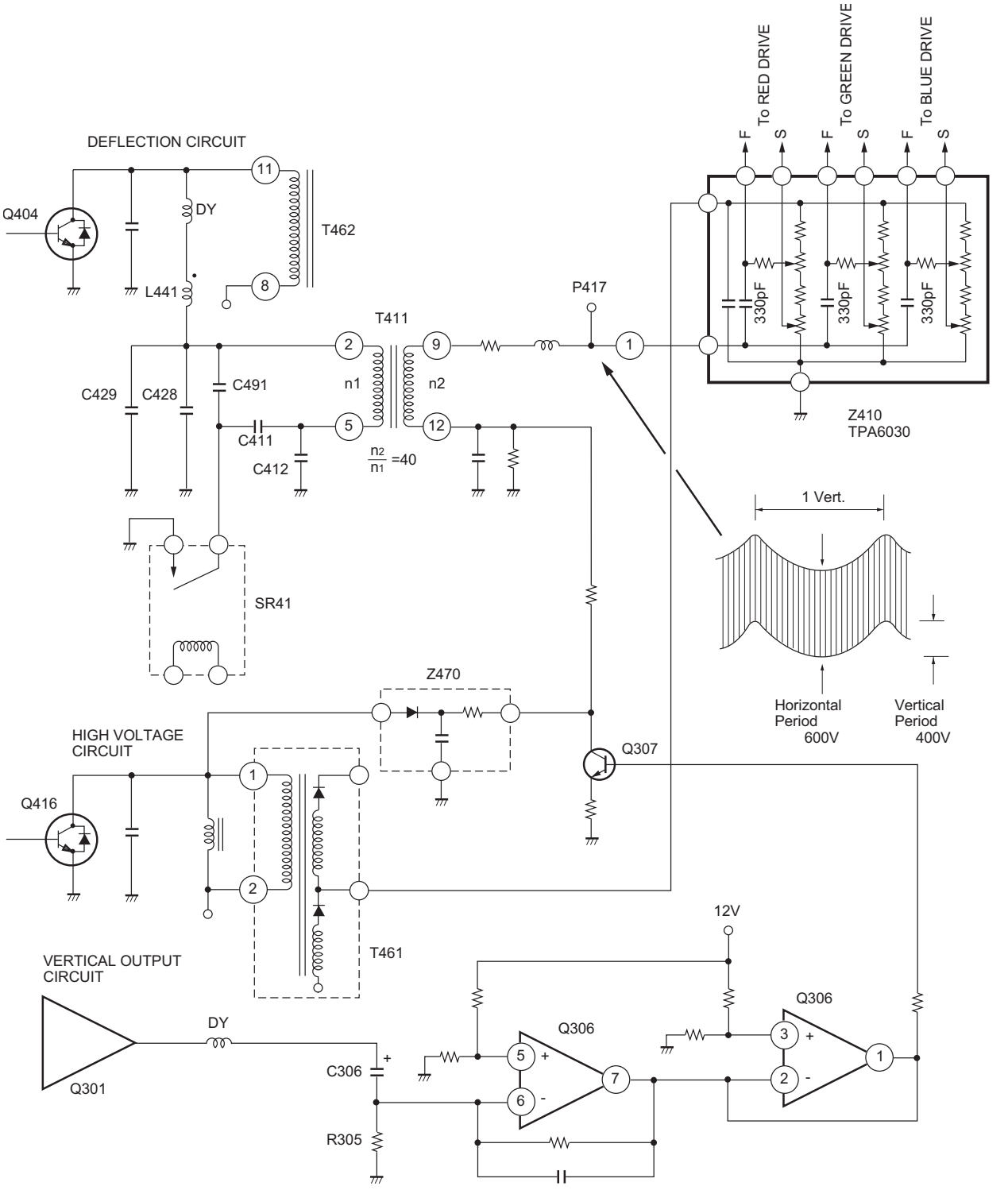


**Fig. 11-1 Dynamic focus circuit diagram**

The parabola voltage generating method of horizontal period is the same as a normal PJTV. The parabola voltage developed across the S character capacitor connected to the deflection yoke in series is stepped up to an approx. 600V by the focus transformer (T411).

In the wide models, to obtain a horizontal linearity with its feature to shrink the center part compressed, S character capacitor is switched to increase its capacity by the relay SR41. In accordance with this, the parabola voltage across the S character capacitor lowers. As a result, in the dynamic focus circuit, swtich is carried out so that C411 is connected to the capacitor C412 in parallel. Furthermore, the parabola voltage added to the primary coil of focus trans T411 is fixed to the same amplitude.

The parabola voltage generating method of vertical famplitude is basically the same as the conventional methd for the PJTVs. However, the amplifier configuration is different a little. In the amplifier circuit using an op. amp Q306 in the first stage, the parabola voltage is generated by mirror-integrating the sawtooth voltage generated at the feed back resistor R305 in the vertical output. This circuit adjusts the amplitude of the parabola voltage to the best value.

Next, in the inverting amplifier circuit, the gain is set to 1 not to change the amplitude and adjusts the DC level of output voltage to the best value. Finally, the parabola voltage generated at the output transistor Q307 collector is added to the return side of the focus trans T411 to superimpose the horizontal and vertical parabola voltages.

The parabola voltage described above is added to the focus pack Z410 and superimposed on the DC voltage extracted from the FTB and adjusted with the the focus VR. Then the voltage is supplied to three CRTs. By the way, teh DC component of the focus voltage of CRT is 27 ± 2%.

The type name of the focus pack Z410 is TPA6030 and the pack is newly developed for this model. The capacitance of the coupling capacitor superimpose the dynamic focus voltage is 100 pF in the conventional TPA6026. On the other hand, it is increased to 330 pF for the TPA6030. This lowers attenuation of parabola voltage of vertical sync. The internal resistance value also differs from the usual one.

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# SECTION XII
# DIGITAL CONVERGENCE CIRCUIT

# 1. OUTLINE

Digital convergence is the circuit which gives output of correcting wave that performs distortion correction and color matching of picture screen. This realizes;

(1) Volume less

(2) Improvement of matching precision

(3) Space saving

(4) Adjustment by remote control

by means of all digital system, which performs better adjustment comparing analog system.

The adjusted data is saved in $E^2$PROM. Memory capacity per one screen is 4k in 60 Hz mode.

# 2. CIRCUIT DESCRIPTION

## 2-1. Configuration

Fig. 12-1 shows a circuit block diagram. The digital convergence unit is composed of QH001 in center position, QH005 PLL circuit for locking input sync signal, QH174 $E^2$PROM for storing data, and D/A converter of QH120, QH121, QH140, QH141, QH160 and QH161 for output of correction wave.

Output waveform from D/A converter of QH120, QH121, QH140, QH141, QH160 and QH161 is amplified and shaped in wave by QH170, QH171 and QH172 to give output from unit. QH001 is equipped with test pattern generator inside to give output of R, G, B and YS signals.

## 2-2. Circuit Operation

(1) When the unit is given with power, RH009 and CH010 perform reset operation and the unit turns in operation ready state.

Two sets of sync signals are input to QH001 and QH005. On basis of sync signal which is input to QH005, the signal is divided in frequency by counter inside QH001, and forms basic clock.

QH001 operates in synchronization with this basic clock and sync signal of set.

(2) QH001 is set up by microcomputer to load data in QH174 to RAM. (60Hz mode 8 x 7 x 3)

(3) On basis of the RAM data, QH001 performs serial data transfer of the specified data to QH120, QH121, QH140, QH141, QH160 and QH161.

In this time, interleaving between RAM data is automatically done by digital filter inside QH001.

(4) Serial data sent from QH001 is, in digital/analog conversion by QH120, QH121, QH140, QH141, QH160 and QH161, converted into analog waveform to be output.

(5) Waveform sent from QH120, QH121, QH140, QH141, QH160 and QH161 is amplified by QH170, QH171 and QH172, and through filter in the next stage, is shaped to be smooth. The correction waveform of R, G, B respectively on horizontal and vertical is obtained.

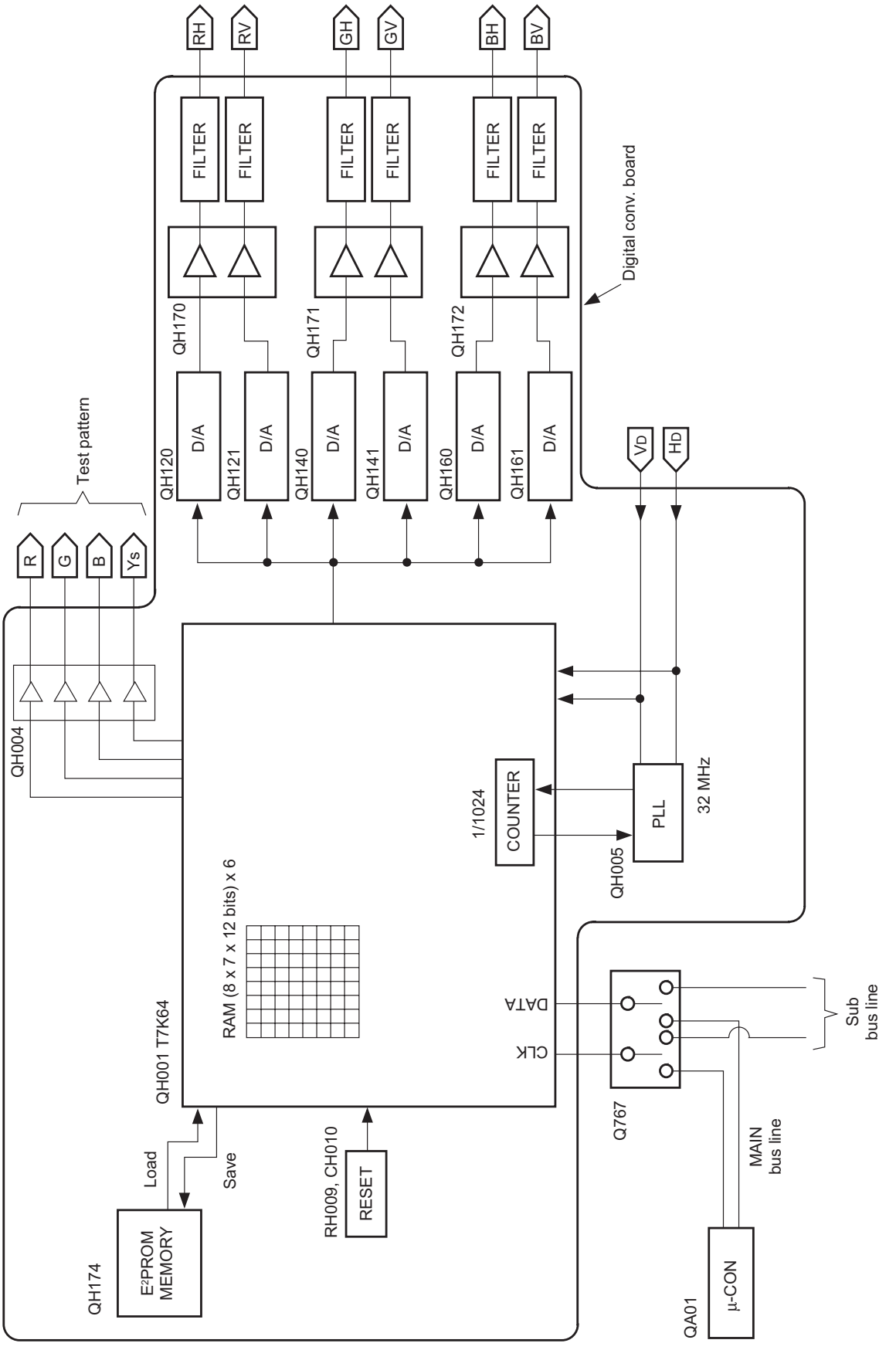
RH
RV
GH
GV
BH
BV
FILTER
Digital conv. board
QH170
QH171
QH172
D/A
QH120
QH121
QH140
QH141
QH160
QH161
VD
HD
Test pattern
R
G
B
Ys
QH004
1/1024
COUNTER
PLL
32 MHz
QH005
RAM (8 x 7 x 12 bits) x 6
QH001 T7K64
DATA
CLK
Sub
bus line
Q767
MAIN
bus line
Load
Save
RH009, CH010
RESET
QH174
E2PROM
MEMORY
QA01
µ-CON

**Fig. 12-1**

# 3. PICTURE ADJUSTMENT

The adjustment is done on 60 Hz mode (NTSC).

## 3-1. Change of Memory ($E^2$PROM)

Memory of QH174 $E^2$PROM is nonvolatile, and adjusted data is stored. Since data in RAM of QH001 is eliminated with power OFF, the RAM is set by soft command of microcomputer QA01 at every power ON. The adjusted data which is obtained from screen-watching is once stored in RAM inside QA01. The whole data in RAM which is corrected on each adjusting point and is changed, is saved into $E^2$PROM (QH174) as a fixed data. The data capacity per one screen requires 4k for 60Hz mode (NTSC).

## 3-2. Service Mode

### 3-2-1. Outline

Service mode is controlled by software of microcomputer QA01, and is one of function of set.

This mode is designed so that ordinary user cannot use this, and special operation is required to use this.

Data change is done by direct shift (cursor display) of adjusting points ; 60 Hz mode (NTSC) 8 x 7 /1 color.

### 3-2-2. To Enter and To Exit

Press MUTE key on remote hand unit twice and keep pressing the key, press MENU key of set console.

Then service data will be displayed on top left of screen. Under the condition, Press “7” key on remote hand unit, and the screen shows crosshatch picture (Later, the first picture). Press again “7” key, and the screen changes to crosshatch + data display (Later, second picture). This time changed data are automatically saved.

Further, press “7” key on remote, the screen returns to original picture.

### 3-2-3. Picture

60 Hz mode (NTSC)

**Correcting point**: Horizontal 8 x Vertical 7
(Arrow marks denote correcting point)

**(1) The first picture**

Crosshatch pattern. Pattern colors are three color display. Cursor is blinking in red. When changed, condition is last memory state.

Cursor is . . . . Data change mode in lighting,
Cursor shifting mode in blinking.

Display color shows the color that data change is possible.

**(2) The second picture**

When entering from the first picture to the second picture, correcting wave of convergence is muted for one second. During this period, the changed data is transferred from RAM QH001 to $E^2$PROM QH174, and saved.

The second picture is indicated with data on top left of the first picture, therefore, convergence cannot be adjusted by this picture.

**Caution:**

- Receive suitable signal for adjustment. Decide the center by cross pattern of static convergence in menu, and adjust convergence from center to circumference.

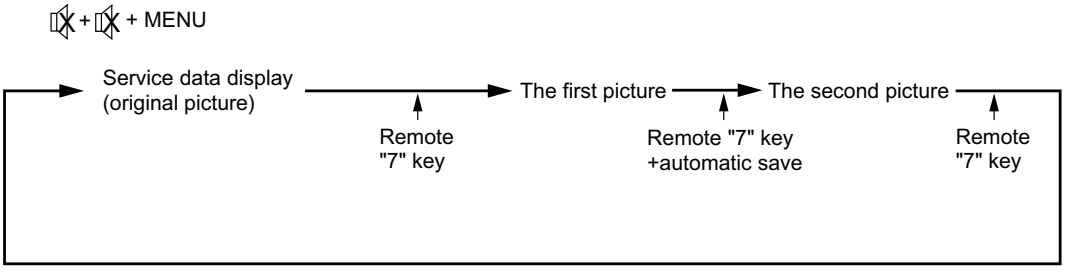


**Fig. 12-2**

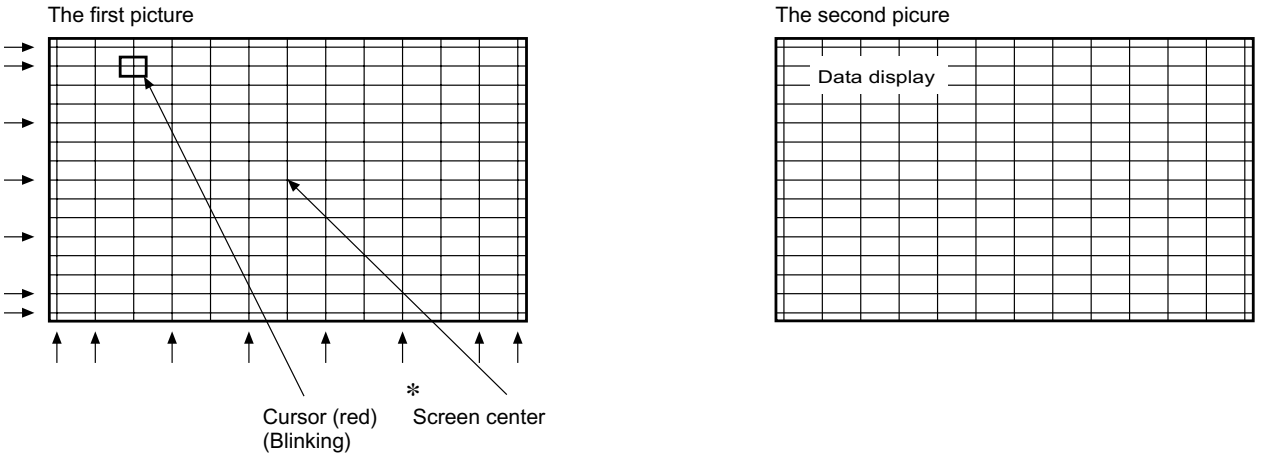


**Fig. 12-3**

# 4. ADJUSTING PICTURE DIMENSION (GREEN PICTURE)

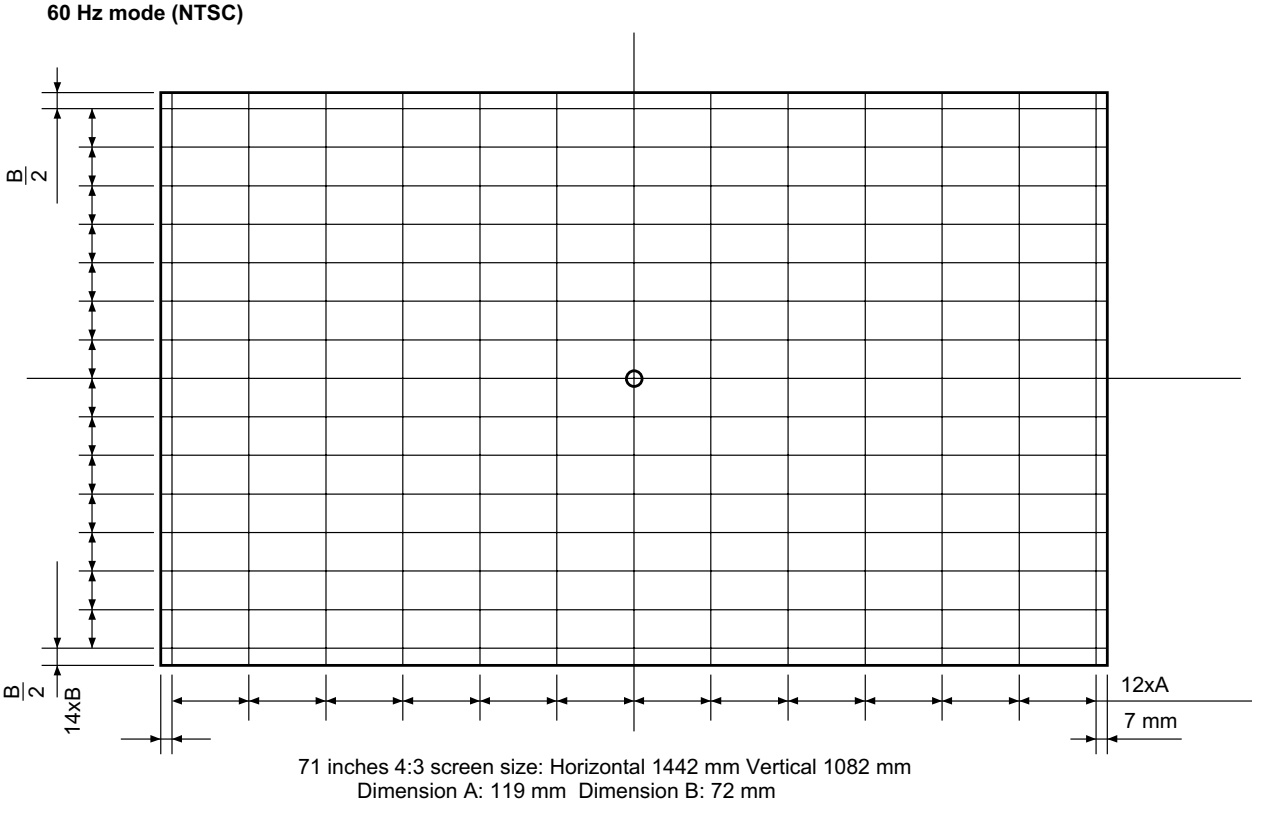


**Fig. 12-4**

# 5. KEY FUNCTION OF REMOTE CONTROL UNIT

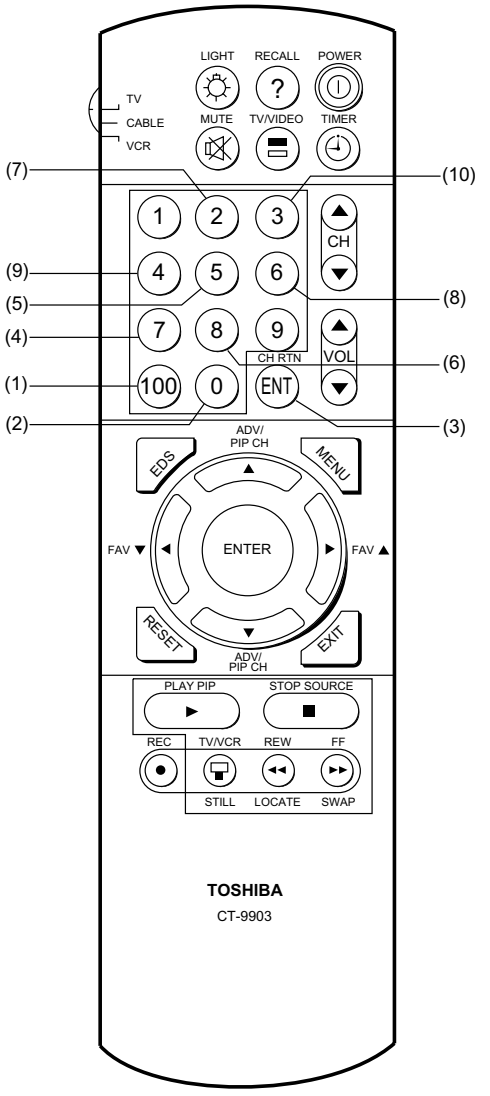


**Fig. 12-5**

(1) 100 key

Red test pattern ON/OFF

(2) 0 key

Green test pattern ON/OFF

(3) ENT key

Blue test pattern ON/OFF

(4) 7 key

Mode picture change-over

(5) 5 key

Cursor shift/data change mode change over

(6) 8 key

Cursor down/adjusting point down

(7) 2 key

Cursor up/adjustment point up

(8) 6 key

Cursor right/adjustment point right

(9) 4 key

Cursor left/adjustment point left

(10) 3 key

Cursor color change

# 6. TROUBLESHOOTING

## 6-1. Adjusting Procedure in Replacing CRT

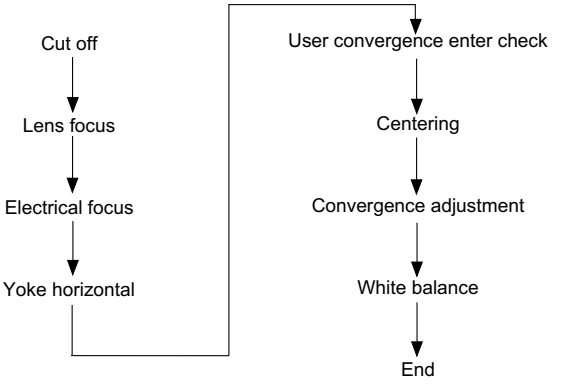


**Fig. 12-6**

## 6-2. Adjusting Procedure in Replacing Convergence Unit/Main Def.

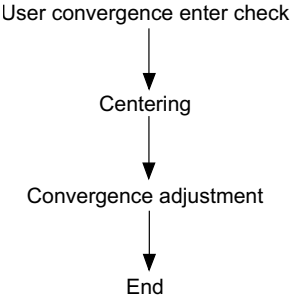


**Fig. 12-7**

# 7. DIGITAL CONVERGENCE CIRCUIT

## 7-1. Outline

The digital convergence circuit develops the correction wave which perform the distortion correction and color matching of the picture on the screen. All the circuit system employ digital system and enable to provide a adequate adjustment environment rather than usual analog circuit system.

The features in the digital convergence circuit are shown below.

- Volumeless
- Fitness accuracy improvement
- Space saving
- Adjustment by a remote controller

The adjusted data is divided in four kinds of data per screen modes and stored in the $E^2$PROM inside the unit. The memory capacity consumed for the operation at the time takes 4 kbits per 1 screen.

First, the adjustment screen appears on the screen by a remote controller operation. Each screen adjustment is carried out so that the dimension is fit to the specified one for each screen.

The unit control is carried out with $I^2C$ format.

## 7-2. Screen Adjustment

In screen adjustment, FULL/STANDARD, WIDE1, WIDE2 and WIDE3 screens are adjusted. To synchronize the adjustment screen frequency to the unit, a broadcasting or a built-in pattern signal of a microprocessor should be received. The adjustment program is memorized in a microprocessor as a preset function of the microprocessor and it is adjustable by a remote controller attached.

The data adjusted through direct inspection calling out the adjustment screen is once written on the RAM inside QH001. Each adjustment point is corrected and all the modified RAM data are stored in the $E^2$PROM as determined data.

The adjustment should be carried out per each screen mode and the adjustment order should be FULL/STANDARD, WIDE1, WIDE2 and WIDE3 mode in order.

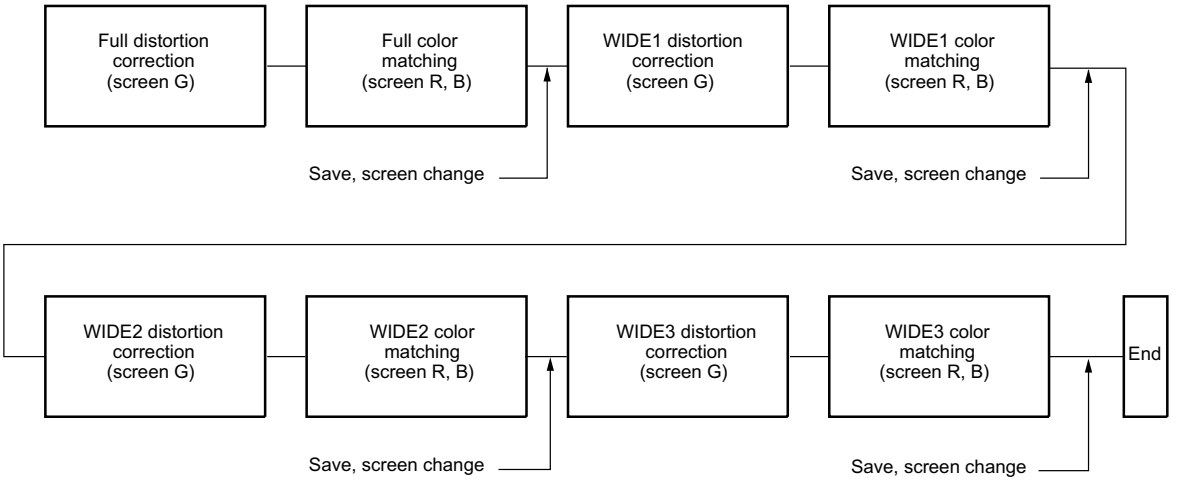


**Fig. 12-8**

## 7-3. Adjustment Procedures when Requesting Convergence Adjustment

### 7-3-1. Adjustment Procedures when Replacing CRT

**Note:**

For details of each adjustment, refer to the applicable items.

The convergence adjustment after replacing a CRT is carried out as follows; the color matching of the CRT pattern not replaced yet should be fit to that of the CRT pattern replaced.

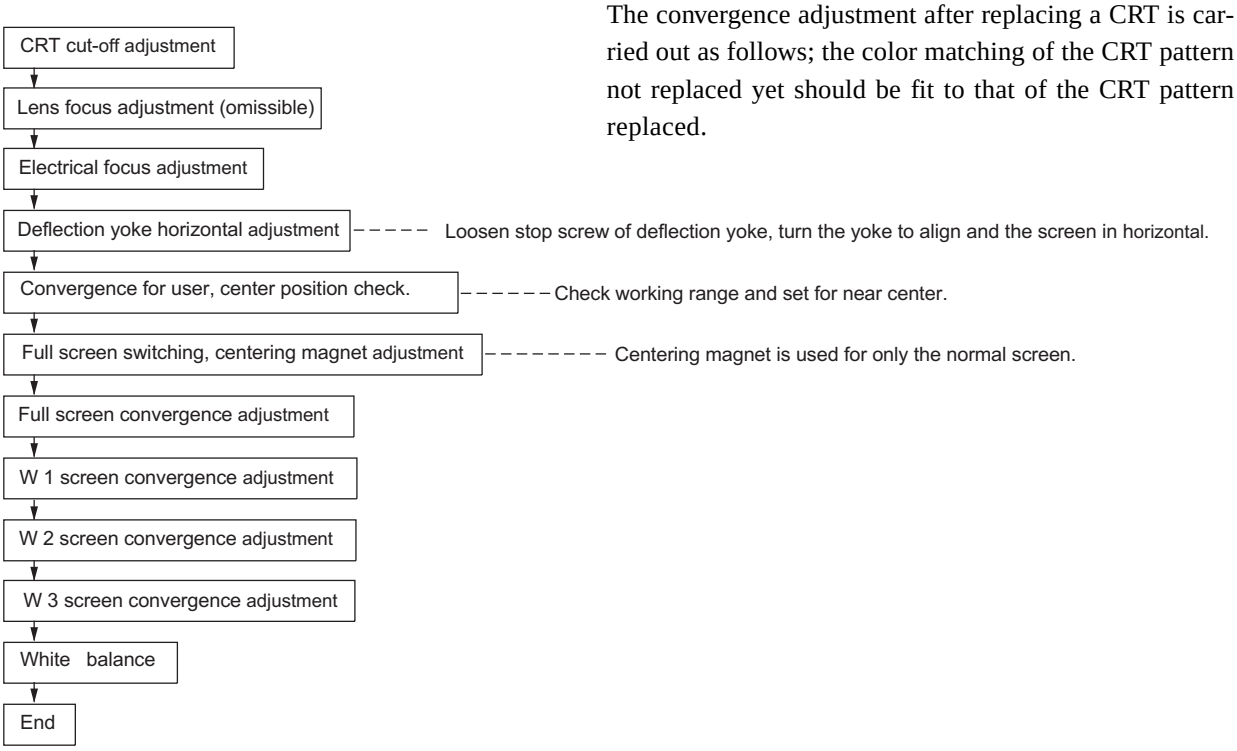


**Fig. 12-9**

### 7-3-2. Adjustment Procedures when Replacing a Convergence Unit and/or a Main Deflection Yoke

**Note:**

For details of each adjustment, refer to the applicable items.

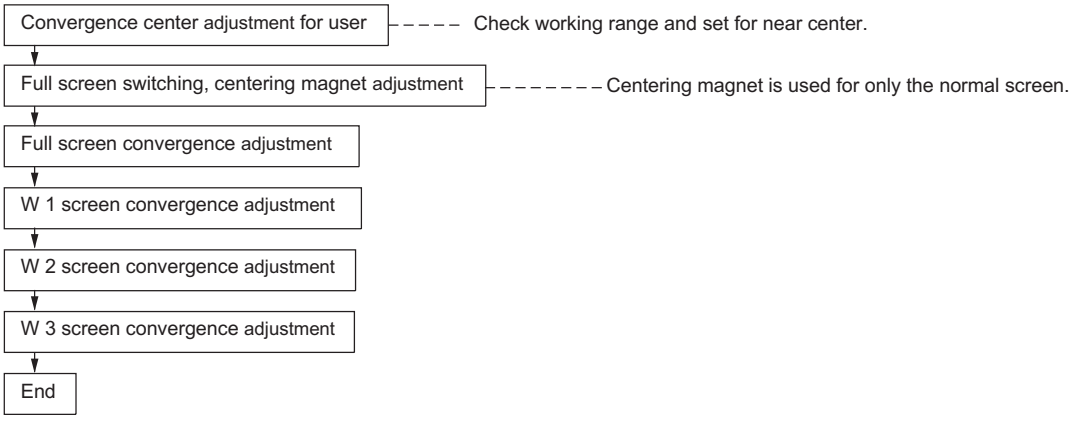


**Fig. 12-10**

### 7-3-3. Adjusting Dimension of Each Picture Screen

65 inches 16:9 screen size:

- Horizontal 1442 mm
- Vertical 810 mm

**(1) FULL**

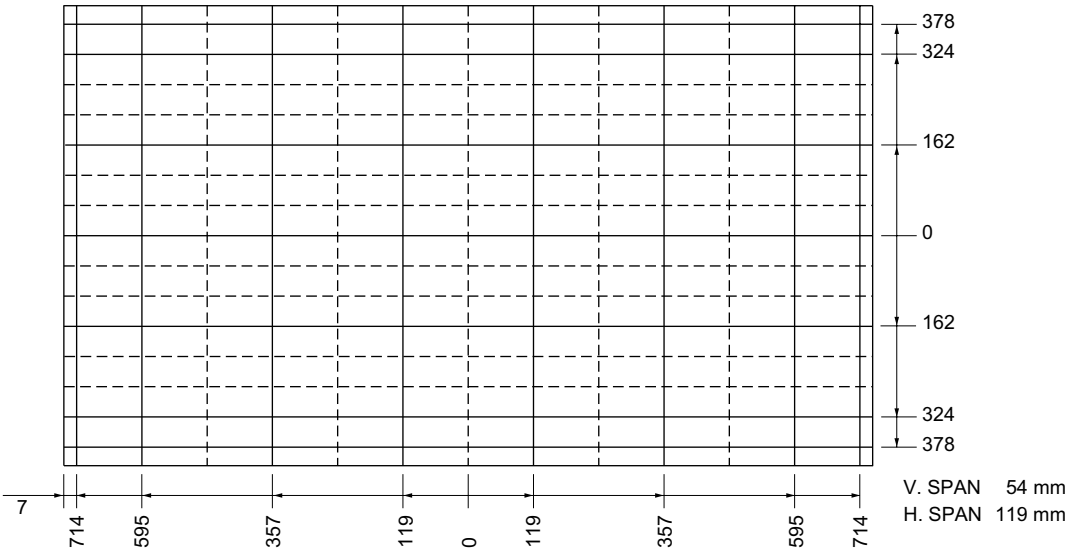


**Fig. 12-11**

**(2) WIDE1**

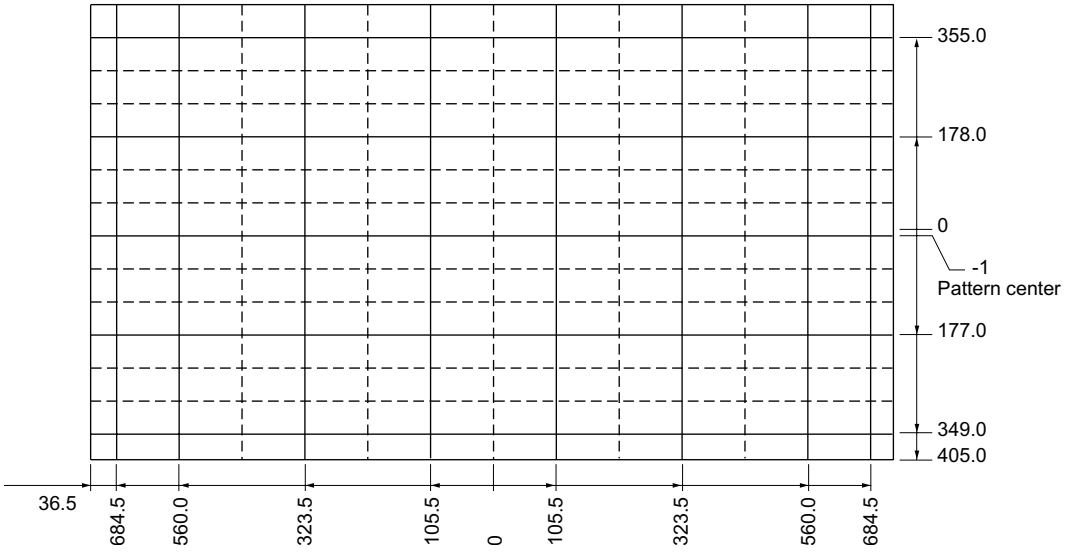


**Fig. 12-12**

**(3) WIDE2**

**Note:**

- In this mode, cursor may be located at out of screen frame. So adjust with care referring cursor position indicated on screen.

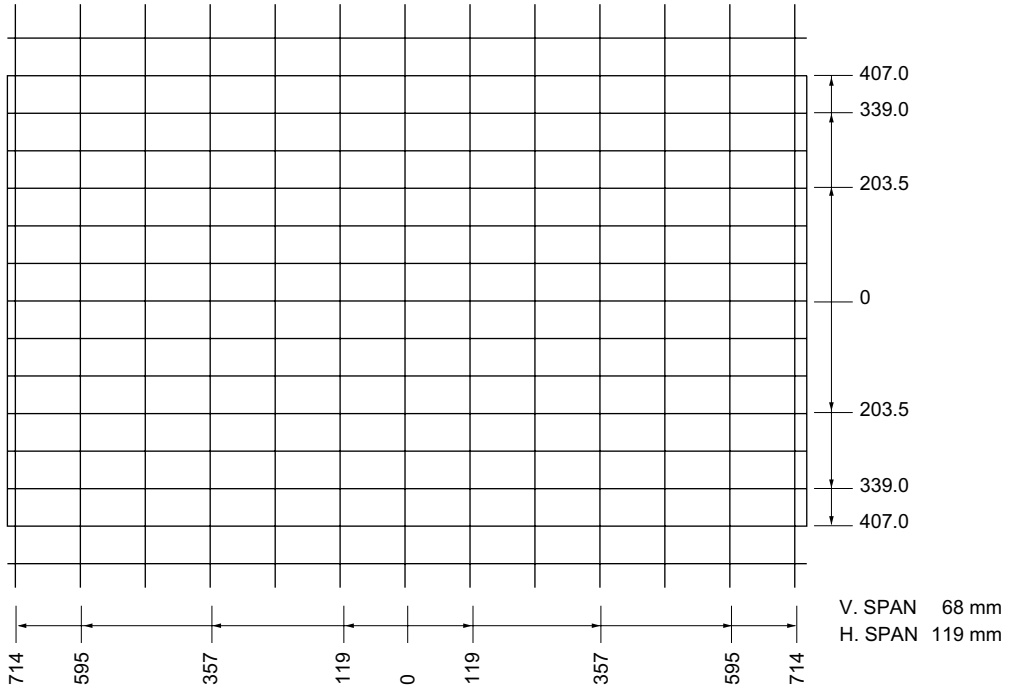


**Fig. 12-13**

**(4) WIDE3**

**Note:**

- In this mode, cursor may be located at out of screen frame. So adjust with care referring cursor position indicated on screen.
- On this screen, convergence pattern center is displayed on screen center, but picture center is indicated at 22 mm up on screen.

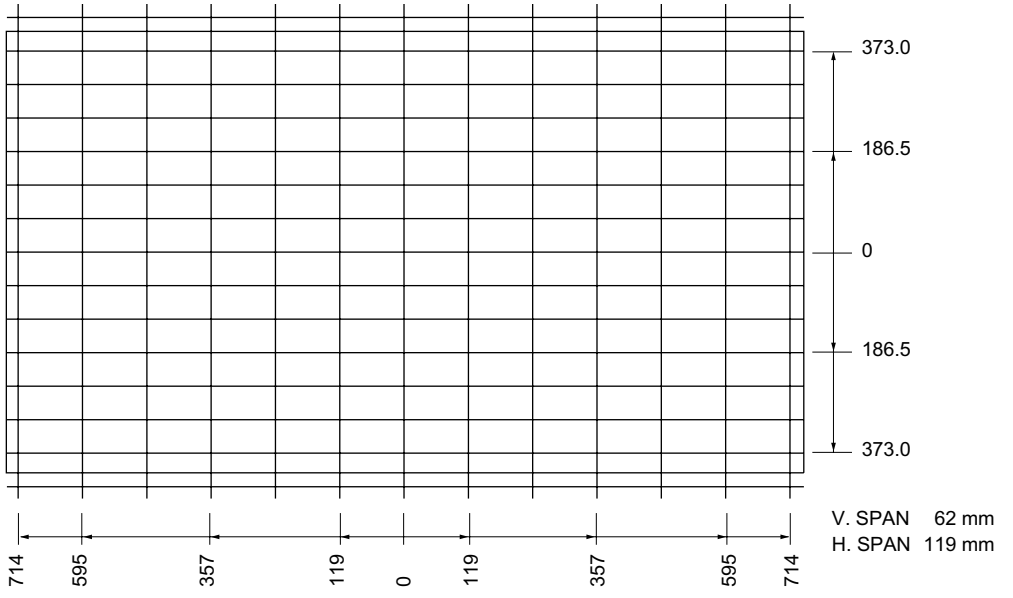


**Fig. 12-14**

# 8. CONVERGENCE OUTPUT CIRCUIT

## 8-1. Outline

This circuit current-amplifies digital convergence correction signal at output circuit, and drives by convergence yoke to perform picture adjustment.

Digital convergence output signal 6ch adjustment is done.

(H-R/G/B) (V-R/G/B)

## 8-2. Circuit Description

### 7-2-1. Signal flow

Signal which is corrected by digital convergence, is output to P708 (V, H R/G/B);

is input to Q751 (V) R/G/B, and is output to P713, P714 and P715;

is input to Q752 (H) R/G/B, and is output to P713, P714 and P715.

### 7-2-2. Over Current Protection Circuit

All currents of Power supply, -21V and +21V are detected to protect CONV-OUT IC from damage due to output short of CONV-OUT.

Current value: Normal ± 21V approx. 900 mA

Detecting current ±21V approx. 2.5A or more protecting operation

### 7-2-3. CONV-OUT Mute

In power-on operation, transistors Q765 and Q766 are made turned ON, and –21V is applied to pin 3 of CONV-OUT IC. These cause mute operation on CONV-OUT.

### 7-2-4. Operation of IC

**(1) Q764 (TC74HC4049P)**

Sync signal which is input from P726B 1VD, 2HD, is, through buffer, supplied to digital convergence P708.

**(2) 3-terminal source**

Q755 (+5V) , Q782 (–5V)

Source for digital convergence

**(3) Q767 (TC4066BP)**

P726B 4 SDAM, 5 SCLM : microcomputer. Busline, through Q767, is input to Digital Convergence P709, and is controlled.

**(4) To adjust from outside of digital convergence :**

Put adjusting jig into 6P socket of P720. Iscs turns from H to L, switch of Q767 is changed over. Then busline from microcomputer is cut off.

P720 3 SCLU, 4 SDAU

Controlled by external adjusting jig.

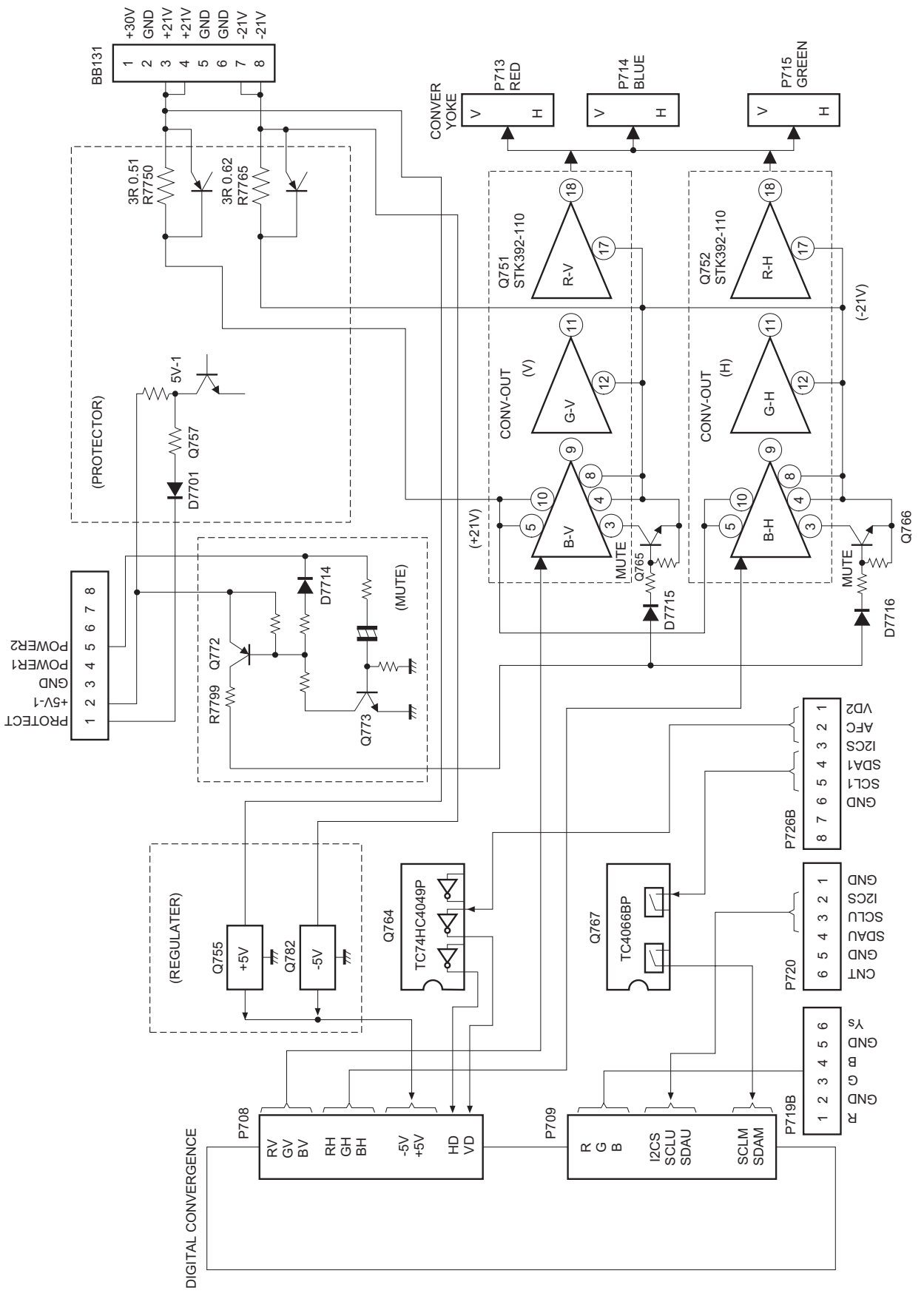


**Fig. 12-15 Convergence block diagram**

# 9. CONVERGENCE TROUBLESHOOTING CHART

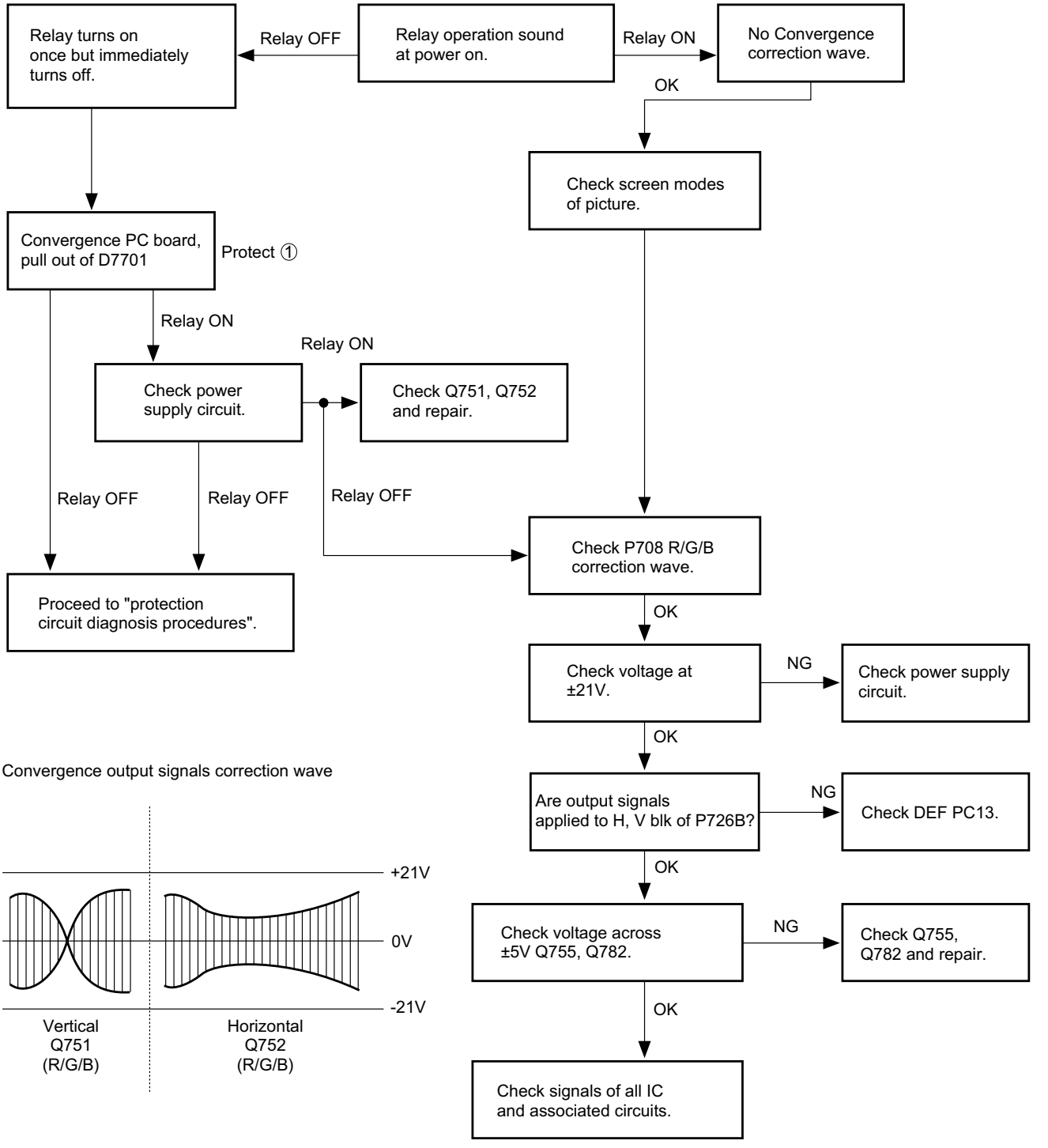


**Fig. 12-16**

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# SECTION XIII
# OPTICAL SECTION

# 1. NECK COMPONENTS

## 1-1. Outline of Components around Neck of the Projection Tube

Fig. 13-1 shows names and mounting locations of neck components around the projection tube.

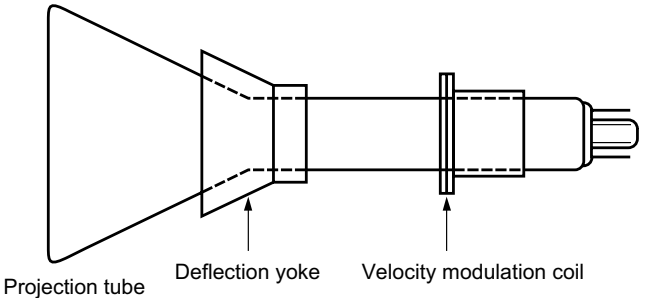


**Fig. 13-1**

## 1-2. Theory of Operation

As The neck components, a deflection yoke (consisting of main yoke, sub-yoke, and centering magnet), and a velocity modulation coil are provided. The main yoke of the deflection yoke consists of a horizontal and vertical deflection coil, and deflects light beams in horizontal and vertical directions. The sub-yoke is called convergence yoke and also consists of a horizontal and vertical coils. The sub-yoke performs distortion correction and color registration according to correction currents supplied from the convergence output circuit. Moreover, a centering magnet consisting of two 2-pole magnets is provided at end of the deflection yoke to adjust the raster position.

## 1-3. Projection Tube

### 1-3-1. TP4688J, TP4880A

**(1) Fluorescent Screen: Flat**

Electrons around peripheral of CRT screen come into collision with the A/B lenses and not used, thus lowering contrast, etc.

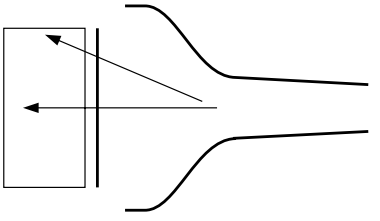

**Fig. 13-2**

**(2) Fluorescent screen: inverted R 350 mm**

Light beams around peripheral of the CRT screen are collected around the center, so, increasing light amount.

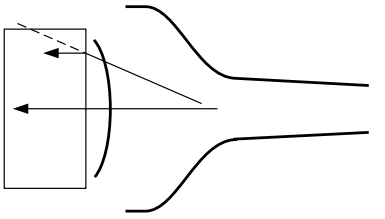

**Fig. 13-3**

### 1-3-2. TP71G90

**(1) Electromagnetic Focus**

Electromagnetic focusing with magnets mounted around the CRT neck.

Since the deflection is carried out by using magnetic field applied from outside of the neck, high deflection power is obtained and focusing quality is high. Moreover, as the coils are mounted outside the neck, so form of the deflection lenses created inside the neck has less distortion, thus the best beam pattern will be obtained.

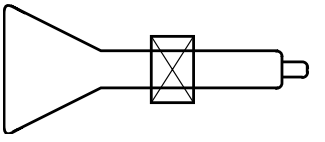

**Fig. 13-4**

**(2) Electrostatic Focus**

High unipotential focus

The best beam pattern is obtained at screen center and screen peripheral by applying parabolic voltages for H and V periods to the focus terminals.

This also assures a flat focusing characteristic on the entire screen.

To obtain clearer pictures, a velocity modulation circuit is provided additionary.

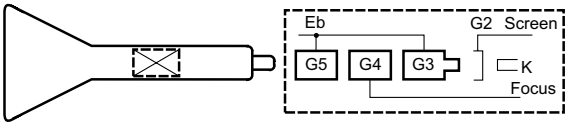


**Fig. 13-5**

# 2. FUNCTION OF KEY COMPONENTS

## 2-1. Outline

The optical system of the TP71G90 consists of a screen, mirros and lens. Description will be given for each block.

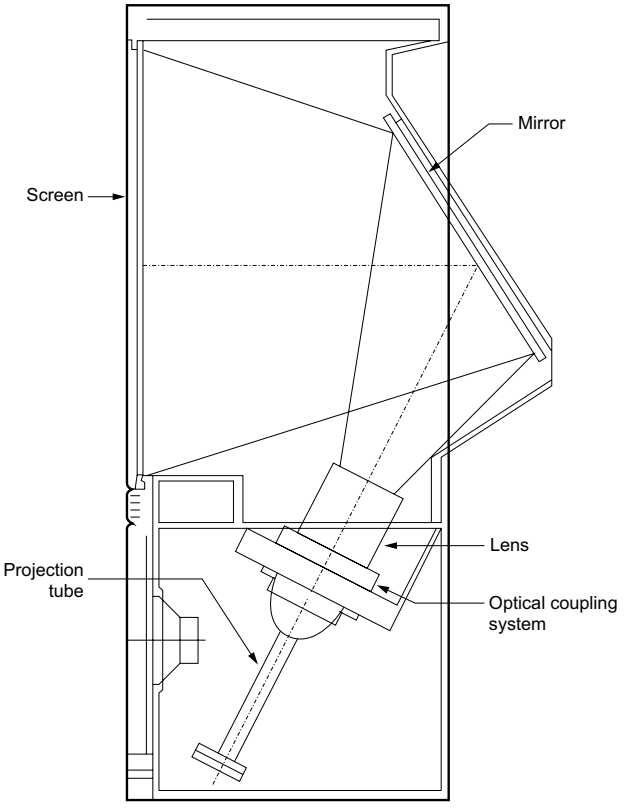


**Fig. 13-6**

## 2-2. Theory of Operation

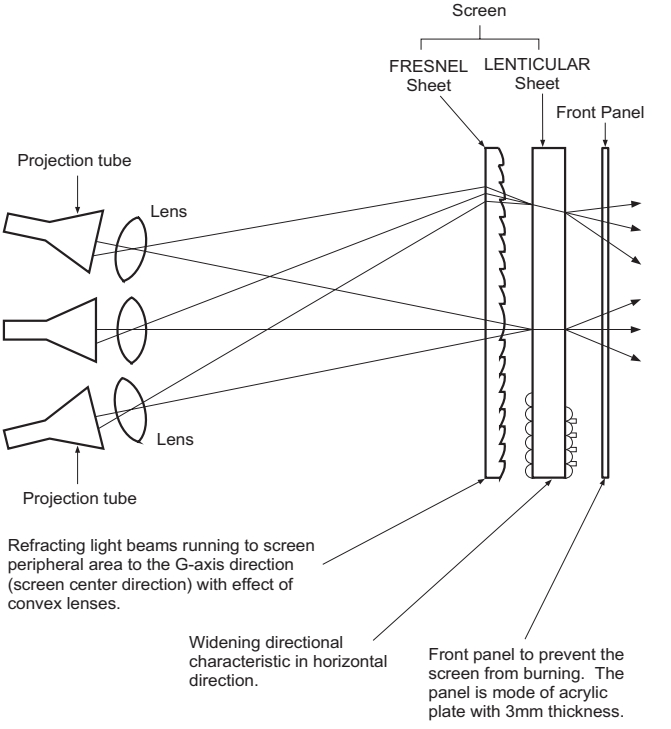


**Fig. 13-7**

## 2-3. Effect of the Screen

### 2-3-1. Effect of Fresnel Sheet

Shape of the lens has been changed to reduce focal length. (This allows reduction on size of product.)

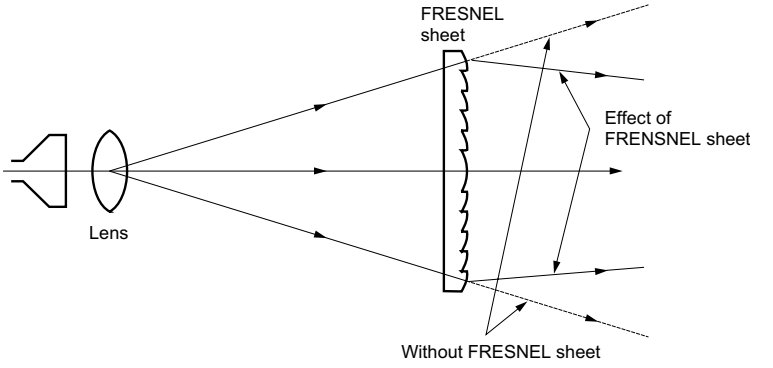


**Fig. 13-8**

### 2-3-2. Effect by LENTICULAR Sheet

If the light enters diagonally, the light diffused in the same way as in parallel light incidence when viewed in front of the TV.

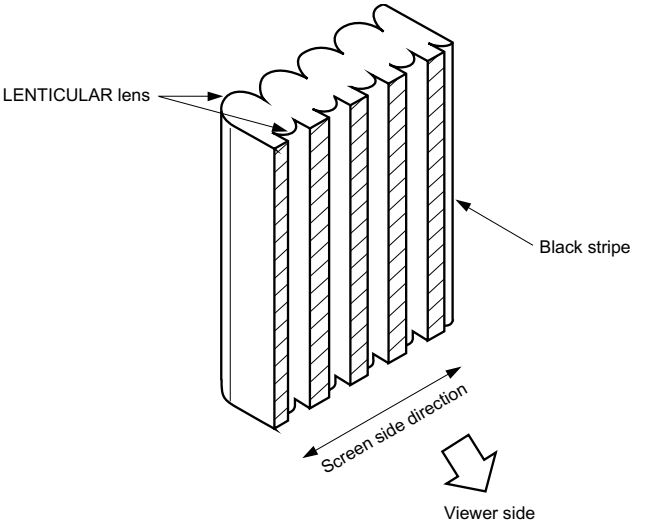


**Fig. 13-9**

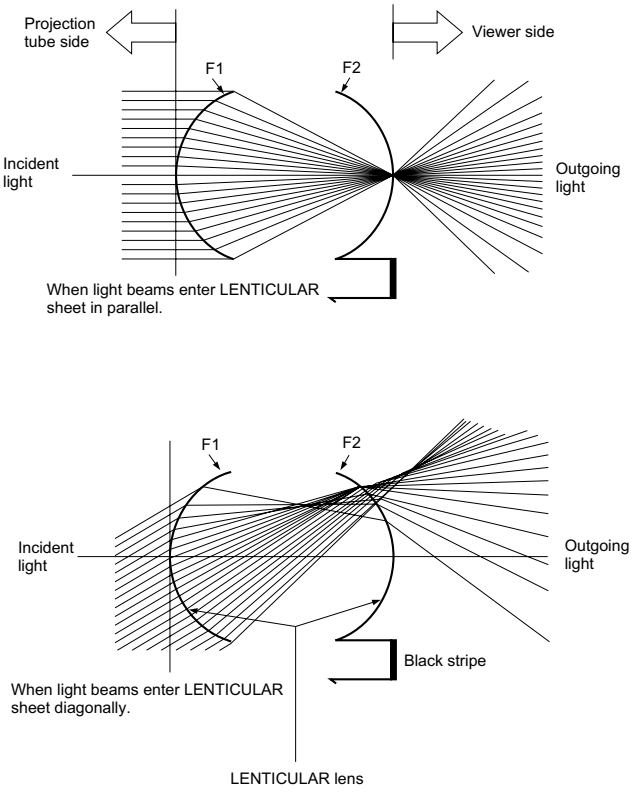


**Fig. 13-10**

## 2-4. Optical Coupling Effect

An object (liquid) with near refraction index of glass is filled between the projection tube and lens to suppress (1) total reflection from the tube, thereby improving the contrast; (2) interfacial reflection to reduce loss of light. Moreover, with the cooling effect of the liquid, power, of the projection tube will be increased.

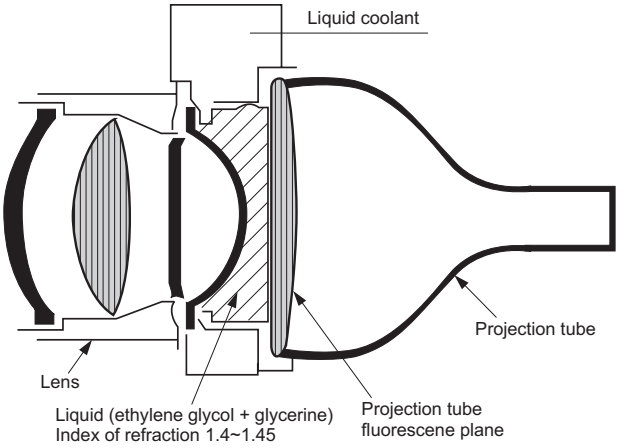


**Fig. 13-11**

### 2-4-1. Optical Coupling Effect

(1) Light beams ① and ② , emitted from the fluorescent surface A advance up to the lens, but light beam ③ returns to the fluorescent surface due to the total reflection.

(2) This extremely lowers the contrast at the fluorescent surface.

With assumption reflection index of air is 1.0 and that of glass 1.5, the angle which causes the total reflection is 41.8°.

That is, the light beams with angle of q higher than 41.8° can not go out the projection tube. The light beams returned to the fluorescent surface reaches 56% of the total beams coming out from A.

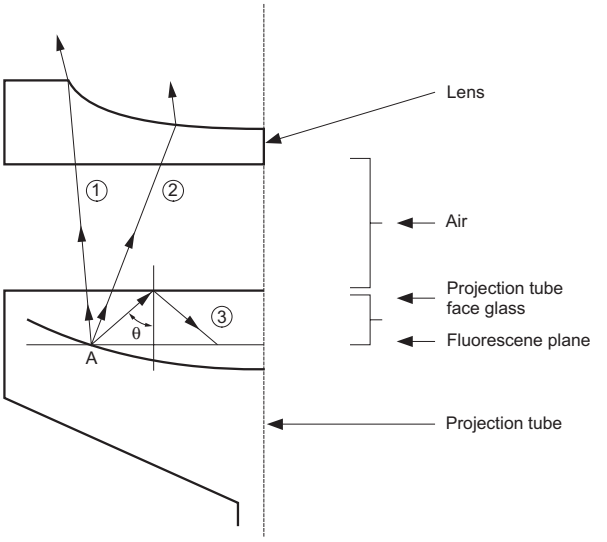


**Fig. 13-12**

## 2-5. Lens

The lens system consists of a main lens (3 pieces of lens), C lens, and the face plate of inverted g CRT (used as a lens), and realizes a short focus optical lens system with less quantity of lens.

With the short focus optical system employed, the depth of the unit is reduced by about 30%, thus making the unit slim and compact.

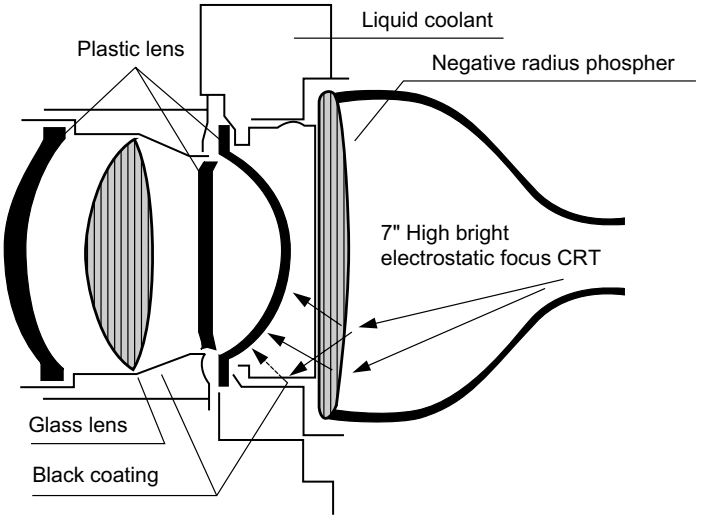


**Fig. 13-13**

**Note:**

- When making adjustments on the neck components, always use dedicated drivers (stainless) made of non magnetic material.

Optical focus will be made according to the procedures shown below. After completion of the electrical and optical focus adjustments, convergence adjustment should be made.

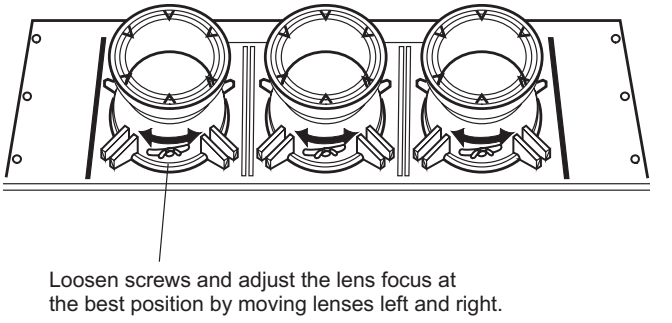


**Fig. 13-14**

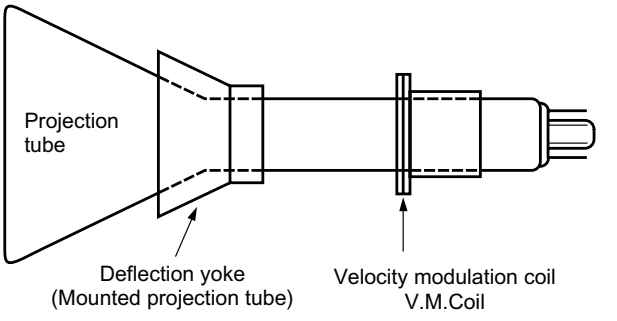


**Fig. 13-15**

## 2-6. Focus Adjustment

(1) Turn on the static convergence switch and receives a cross character signal.

(2) For easy adjustment, project one color to be adjusted at a time on the screen. (Other colors can be interrupted by putting caps on the lens.)

(3) Turn the electrical focus volume for the color to be adjusted clockwise or counterclockwise so that the focus at center of the cross character shows the best.

(4) Loosen screws securing the lens and move the lens toward left and right until the best focus is obtained at center of the cross character.

(5) Repeat steps 3 and 4 to obtain the best focus. Finally, secure the screws.

(6) Perform the convergence adjustment according to the convergence adjustment method.

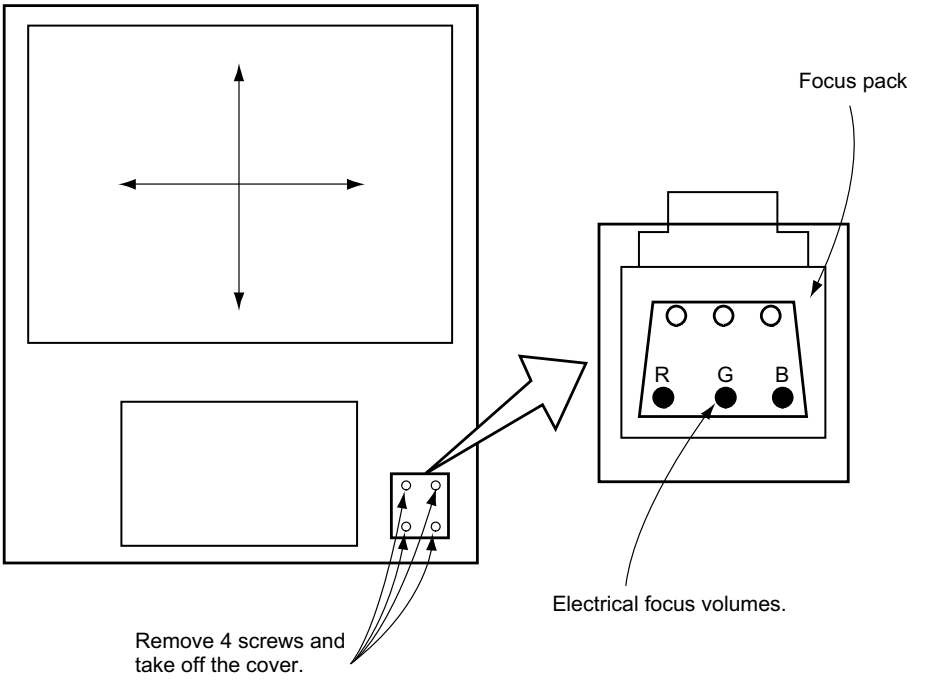


**Fig. 13-16**

# SECTION XIV
# POWER SUPPLY CIRCUIT

# 1. OUTLINE

The Power PC board has three power supplies,

(1) STANDBY

(2) POWER-1

(3) POWER-2.

It has the PROTECT function which works when any error occurs.

## 1-1. STANDBY Power Supply

- Standby transformer and series regulator system.
- +5V – 1 always supplied to the microcomputer.

## 1-2. Power-1

- RCC (Ringing choke converter) system
  6 outputs
- Main +B +148V
- Lo +B, +35V, +15V, +11V, +7V – 1, +7V – 2, +11V:

  For the 9V channel regulator IC in CONV/SIGNAL PC board

  +7V – 1:

  For the 5V channel regulator IC in CONV PC board

  +7V – 2:

  For the HEATER 6.3V/5V channel regulator IC in CONV PC board

## 1-3. Power-2

- Current resonation system: 3 outputs
- ±21V: For the CONVERGENCE UNIT
- +35V: For the AUDIO AMP

## 1-4. Protect Function

This stops the AC power supply of POWER-1 and POWER-2 and protects the circuit when the voltage and current of the DEF CONV POWER circuit becomes abnormal.

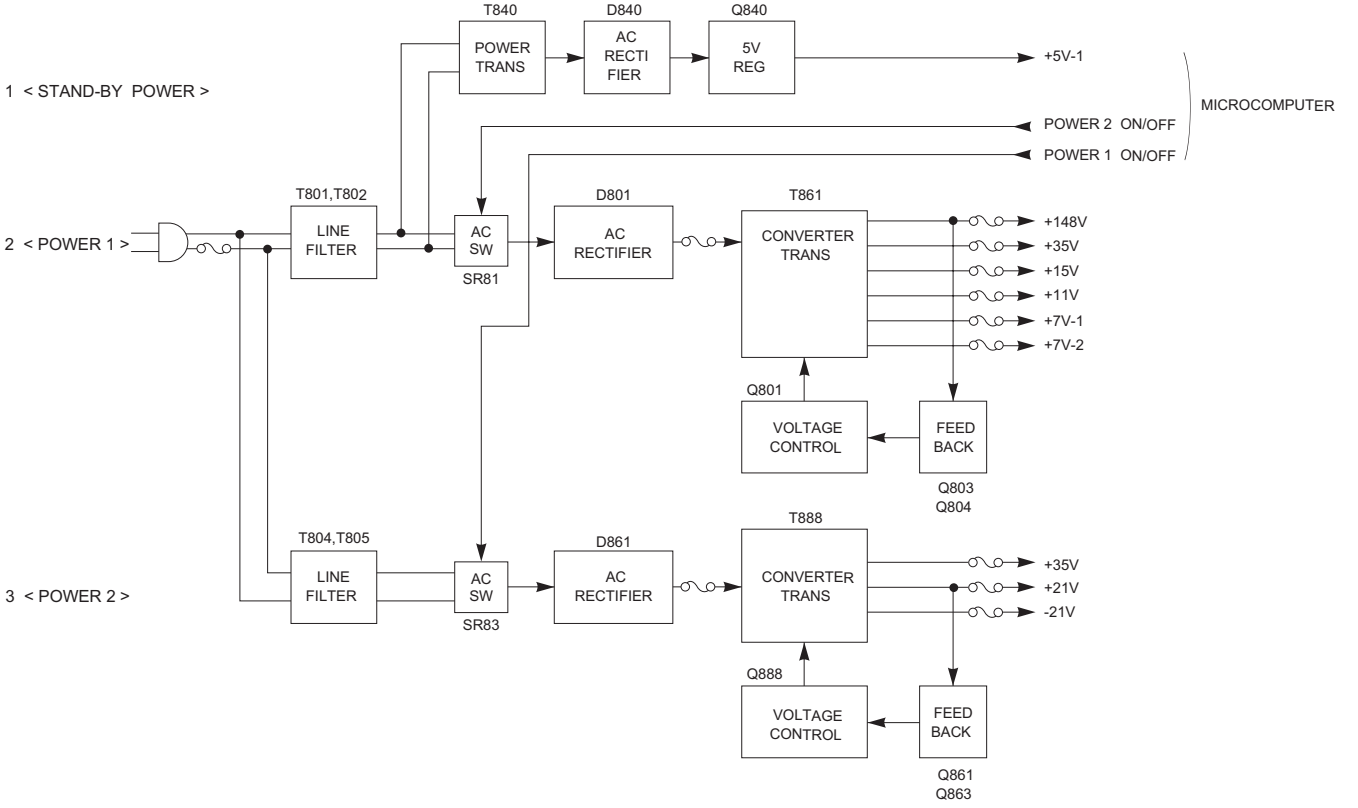


**Fig. 14-1 Power supply PC board system diagram**

## 1-5. Power Supply Line Connection Diagram

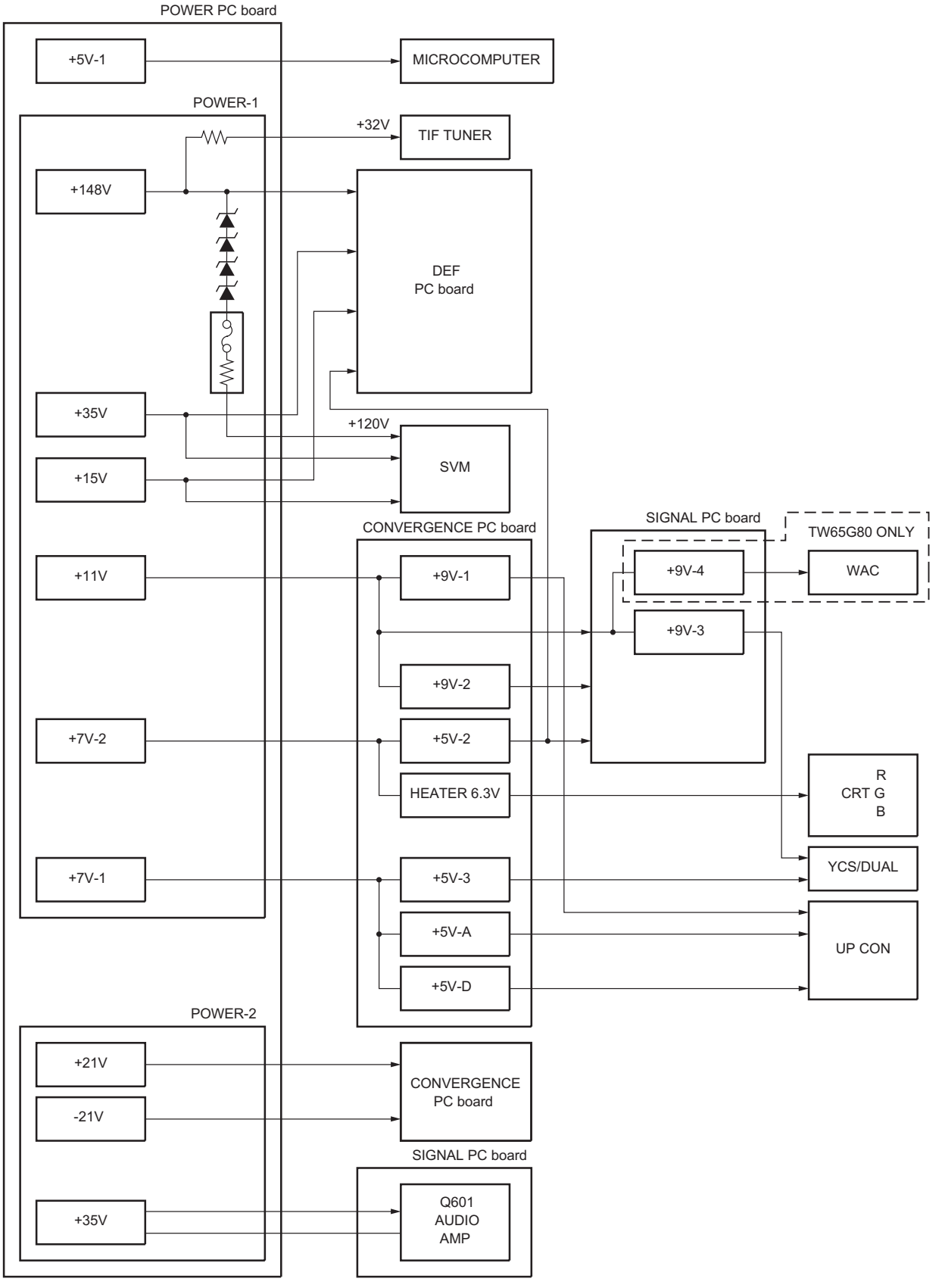


**Fig. 14-2**

## 2. STANDBY POWER SUPPLY

The standby power supply comprising a standby transformer and a +5V – 1 series regulator. It is always supplied to the microcomputer.

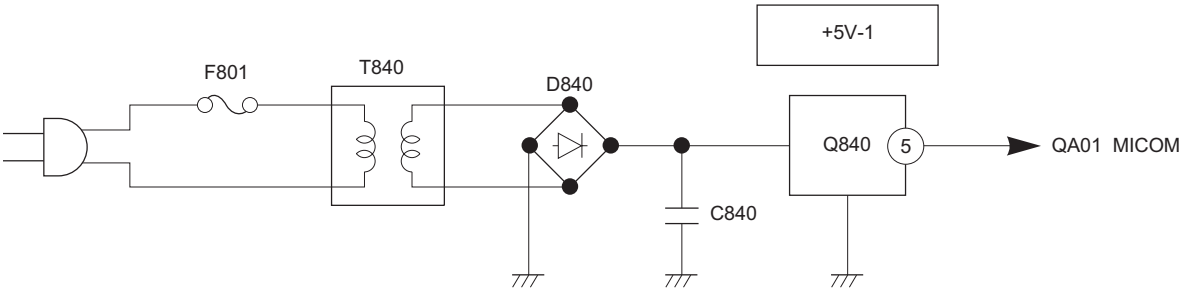


**Fig. 14-3**

## 3. POWER-1

### 3-1. Block Diagram

The block diagram of the power IC is shown below.

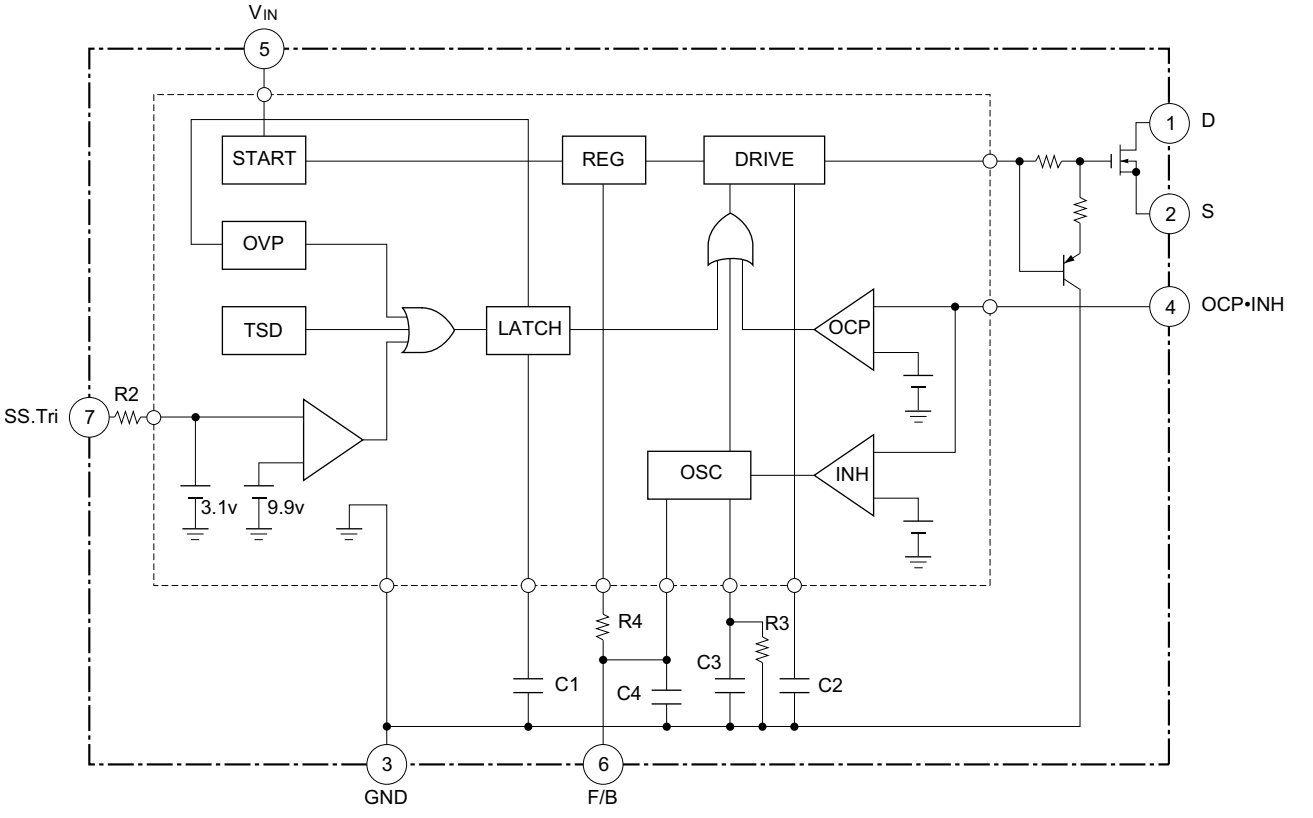


**Fig. 14-4 Q801 STR-M6811A block diagram**

**Table 14-1 Pin functions**

| Pin No. | Symbol | Name | Function |
|---|---|---|---|
| 1 | D | Drain terminal | MOS FET drain |
| 2 | S | Source terminal | MOS FET source |
| 3 | GND | Grounding terminal | Grounding |
| 4 | OCP/INH | Overcurrent terminal | Overcurrent detection signal input |
| | | Inhibit terminal | OFF time cyclic operation signal input |
| 5 | $V_{IN}$ | Power supply terminal | Control circuit power supply input |
| 6 | F/B | Feedback terminal | Constant voltage control signal input |
| 7 | SS/Tri | Latch trigger terminal | Latch circuit operation signal input |
| | | Soft start terminal | Soft start voltage output |

## 3-2. STR-6811A Pins and Peripheral Circuit Operation

### 3-2-1. $V_{IN}$ Terminal (pin 5) - Start Circuit

The start circuit detects the voltage at the $V_{IN}$ terminal (pin 5) to start/stop operation of the control IC. The power supply ($V_{IN}$ terminal input) of the control IC uses the circuit (shown in Fig.14-5). When the $V_{IN}$ terminal voltage reaches 22.5V TYP by charging C825 with the start resistors R803 and R802 when the power supply is started, the control circuit is activated by the start circuit.

As shown in Fig.14-6, before the control circuit is activated, the circuit current is suppressed to 100 µA maximum ($V_{IN}$ 16V Tc25℃), and is supplied with R803 and R802. After the control circuit is activated, the voltage generated in the auxiliary winding $N_D$ is smooth rectified with D805 and C825 and is supplied to the $V_{IN}$ terminal, pin 5. Since this voltage does not reach the constant voltage immediately after the control circuit is activated, the $V_{IN}$ terminal voltage begins to drop.

But, as the operation stop voltage has been set to 16.2V (maximum), while this voltage is dropping, the auxiliary winding voltage reaches the set value and the control circuit continues operation. Fig. 14-7 shows the $V_{IN}$ terminal voltage waveform at starting.

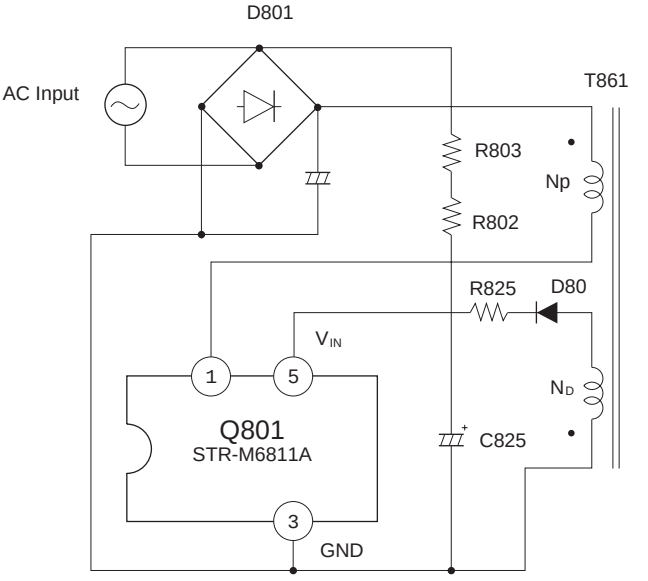


**Fig. 14-5 Start circuit**

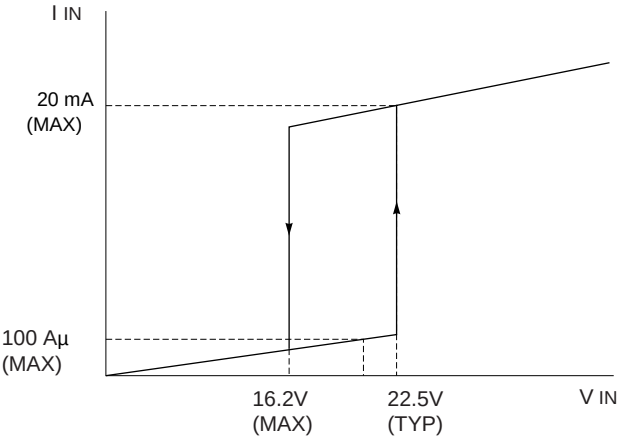


**Fig. 14-6 $V_{IN}$ terminal voltage/Circuit current**

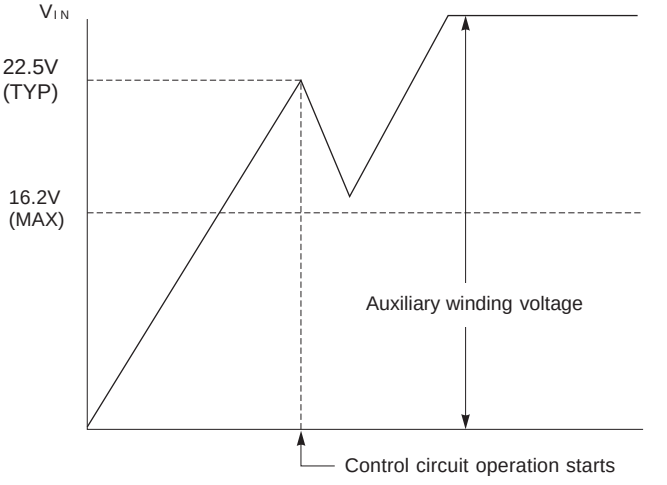


**Fig. 14-7 $V_{IN}$ terminal voltage waveform at starting**

### 3-2-2. F/B Terminal Voltage (pin 6)/Oscillator/ Constant Voltage Control Circuit

As shown in Fig. 14-8, the oscillator utilizes the charging/ discharging of C3, C4 of the hybrid IC, generating a pulse signal to turn on and off MOS FET. The constant voltage control when forming a switching power supply is performed by changing the ON and OFF time except the PRC operation.

Fig. 14-9 shows the oscillator operation when the hybrid IC operates independently (without F/B and OCP/INH signals). When MOS FET is ON, C3 is charged to the regulated voltage (approx. 4.5V, Ta = 25℃). C4 starts charging from almost 0V through R4, and the voltage on its both ends increases along the slope determined by the charging time constant of C4 and R4. When the voltage at both ends of C4 reaches 0.75V (Ta = 25℃), the oscillator output is reversed and MOS FET turns off. At the same time, C4 is rapidly discharged with the internal oscillator circuit, and the voltage at both ends becomes almost 0V. When MOS FET turns off, C3 starts discharging with R3, and the voltage at both ends decreases along the slope determined by the discharging time constant of C3 and R3. When the voltage at both ends of C3 decreases to 2.7V, the oscillator output is reversed again and MOS FET turns on. MOS FET continues turning on and off by repeating the above operation. The ON time determined by the above C4 and R4 is the maximum ON time of MOS FET, and the OFF time determined by C3 and C4 is the fixed OFF time (without INH signal).

Fig. 14-10 shows the oscillator operating waveform (with PRC operated) at the time of constant voltage control. The ON time is controlled with the photocoupler connected to the F/B terminal (pin 6) as the circuit of Fig. 14-8 by flowing the current equivalent to the output signal of the output voltage detection circuit (error amplifier) provided in the secondary side output, and by changing the C4 charging current. As the power supply AC input voltage is higher and the load current is smaller, the F/B terminal flowing current becomes larger and the ON time becomes shorter.

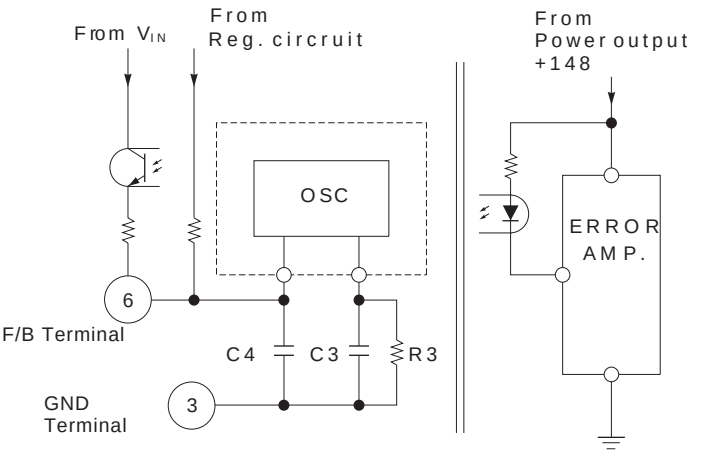


**Fig. 14-8 Oscillation circuit**

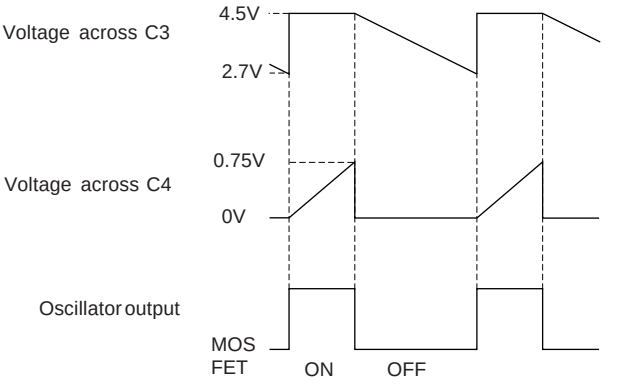


**Fig. 14-9 Oscillator operating waveform (without F/B, OCP/INH signals)**

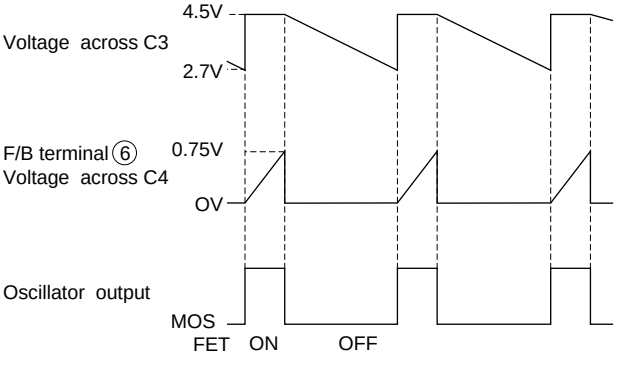


**Fig. 14-10 Oscillator operating waveform (with F/B signal)**

### 3-2-3. OCP/INH Terminal (pin 4) Function

The OCP/INH terminal input signal is used as an input for Comp.1 ($V_{OCP}$) and Comp.2 ($V_{INH}$) in the control IC of Fig. 14-11.

**(1) OCP Function (Switching Current Control)**

Detects the drain current peak value of MOS FET at every pulse, and reverses the drive output (pulse impulse system). Fig. 14-12 shows the overcurrent detection circuit.

The drain current of MOS FET is detected by connecting Rocp (R827/R828) between the source terminal (pin 2) and GND terminal (pin 3) of MOS FET, and applying the drop voltage to the OCP/INH terminal (pin 4). The threshold voltage $V_{OCP}$ of OCP/INH terminal is about 0.5V (TYP)(Ta = 25°C) against GND. This detection voltage is set by the comparator, and the drift of detection voltage due to a temperature change is almost 0V showing the stable characteristic against a temperature.

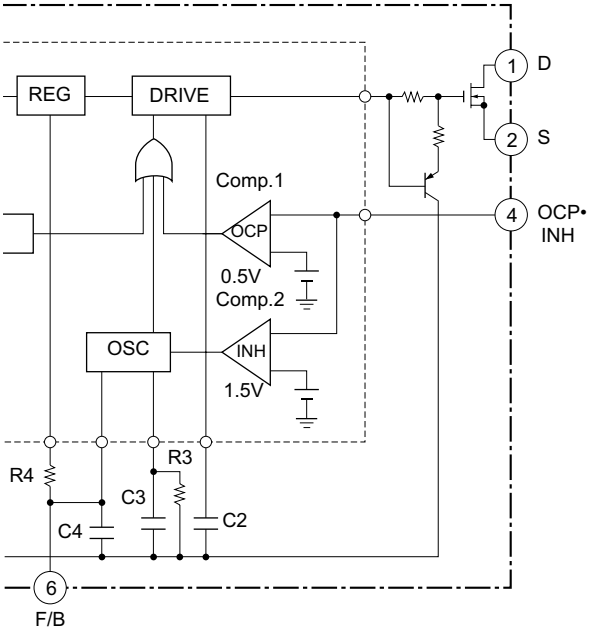


**Fig. 14-11 OCP/INH terminal circuit**

**(2) INH Function (OFF Time Control)**

Figs. 14-13 and 14-14 show the relationship between the voltage of OCP/INH and the oscillator operation. By applying the voltage signal (pseudo resonance operation signal) greater than the Comp.2 threshold voltage ($V_{INH}$) to the OCP/INH terminal (pin 4) when MOS FET is OFF, the OFF time (approx. 50 µs) which has been determined by the product of C3 and R3 is made the OFF time synchronizing with the pseudo resonance operation signal. The threshold voltage ($V_{INH}$) of Comp.2 is set to about 1.5V (TYP)(Ta = 25°C) . When the voltage at the OCP/INH terminal (pin 4) reaches $V_{INH}$, the Comp.2 output is reversed. At this time, the voltage at both ends of C3 starts charging and increases to 4.5V in a moment. Unless the voltage at the OCP/INH terminal drops to lower than $V_{OCP}$, the drive output continues OFF. As this detection voltage is also set by the comparator as $V_{OCP}$, the detection voltage drift due to a temperature change is almost 0V.

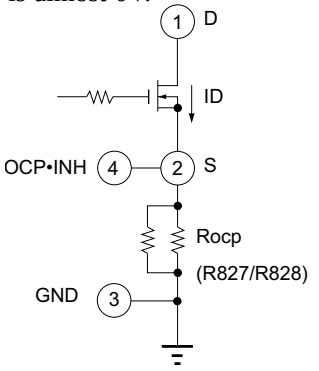


**Fig. 14-12 Overcurrent detection circuit**

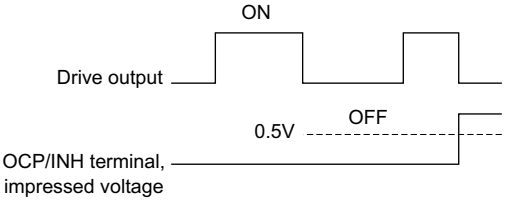


**Fig. 14-13 Oscillator waveform with Vocp operating**

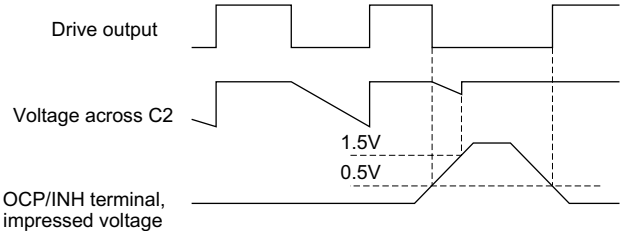


**Fig. 14-14 Oscillator waveform with VINH operating**

### 3-2-4. Drive Circuit

This circuit receives the pulse signal from the oscillator to charge/discharge the capacitor between the gate source of MOS FET.

The STR-M6811A employs the proportional drive system; the drain current ID flows about 1µsec (Ta = 25°C) after the pseudo resonance drops to lower than 0.5V (TYP), reducing the ON Loss and switching noise caused by the surge current when the MOS FET turns ON.

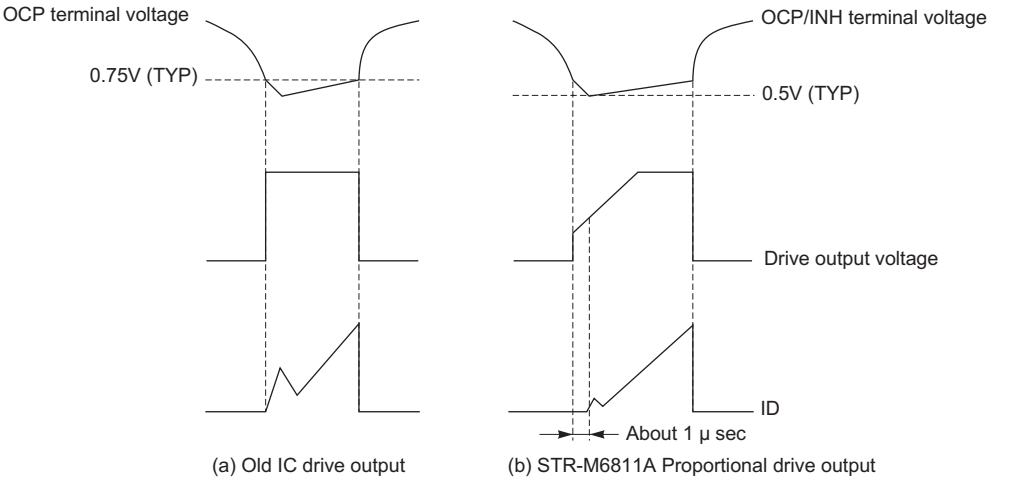


**Fig. 14-15 Drive output voltage and drain current waveform**

### 3-2-5. SS/Tri Terminal (pin 7) Soft Start Circuit

The drain current to flow in MOS FET when the power is turned on can be suppressed with C818 and R811 of the SS/Tri and OCP terminals as shown in Fig. 14-16. Fig. 14-17 shows the drain current waveform at starting. When the power is turned on, the start circuit is activated as described before. When the start circuit is activated, 3.1V is supplied from the Reg circuit to the SS/Tri terminal. With this voltage, a charging current flows in C818 and the OCP/INH terminal (pin 4) potential increases.

As the OCP/INH terminal potential changes proportional to the C818 charging potential, it decreases as the time passes. When the power supply is turned on, the OCP circuit is activated by the voltage drop of Rocp (R827/R828) due to the ID flowing in MOS FET and the C818 charging current. As the drain current of MOS FET gradually increases when the power is turned on, a stress of MOS FET is suppressed.

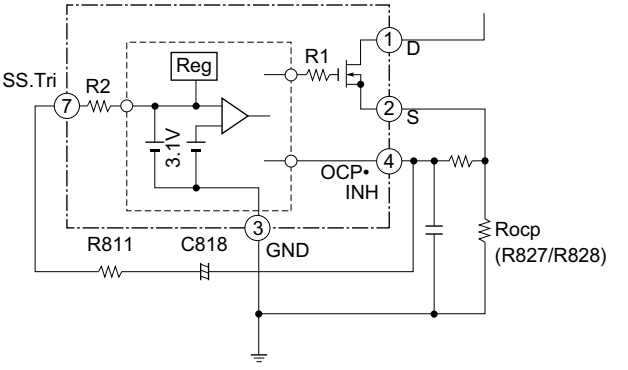


**Fig. 14-16 Soft start circuit**

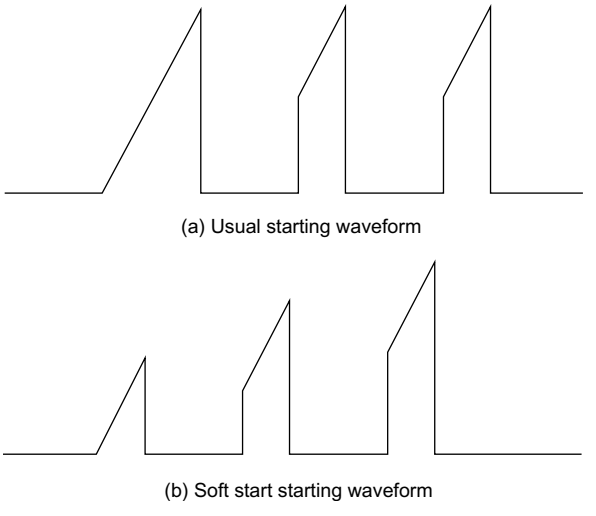


**Fig. 14-17 Drain current waveform at starting**

### 3-2-6. Latch Circuit

This circuit holds the drive output low and stops operation of the power supply circuit when the overvoltage protection (OVP) circuit or the overheat protection (TSD) circuit works and when an external signal over 9.9V (TYP) is applied to the SS/Tri terminal (pin 7).

The hold current of the latch circuit is set to 600 µA maximum as described before, and if a current greater than 700 µA is applied to the $V_{IN}$ terminal through the start resistor, the drive output can be held stopped. To prevent a malfunction due to a noise, a delay time is set with C1 with a built-in hybrid IC.

So the latch circuit is activated when the OVP or TSD circuit operates and when an external signal input continues for about 10µ second. The constant voltage power supply circuit (Reg) in the control circuit operates even if the latch circuit is activated, and the circuit current is held high.

Therefore, the $V_{IN}$ terminal voltage rapidly drops. When the $V_{IN}$ terminal voltage drops to lower than the operating stop power supply voltage (15.1V (TYP)), the circuit current decreases, and the $V_{IN}$ terminal voltage begins to increase. When it reaches to the operating start supply voltage 22.5V (TYP), the circuit current increases again and the $V_{IN}$ terminal voltage decreases. Therefore, when the latch circuit operates, the $V_{IN}$ terminal voltage fluctuates between 15.1V (TYP) and 22.5V (TYP) as shown in Fig. 14-18, preventing abnormal increase of the $V_{IN}$ terminal voltage. The latch circuit is reset by decreasing the $V_{IN}$ terminal voltage to 8.6V (TYP) or lower. To resume the latch circuit, turn off the AC power input or turn the power switch ON/OFF.

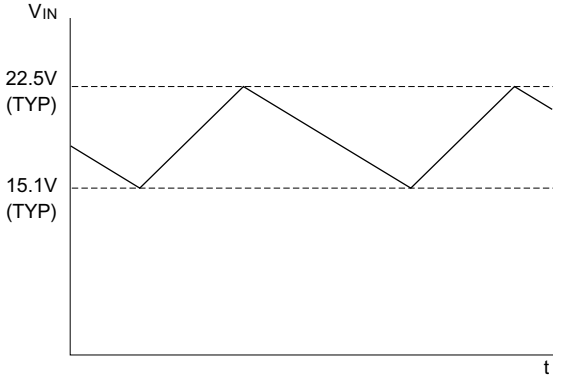


**Fig. 14-18 $V_{IN}$ terminal waveform with latch circuit operation**

### 3-2-7. Overheat Protection Circuit

This circuit actuates the latch circuit when the hybrid IC frame temperature exceeds 125°C (minimum).

Detection of temperature is actually performed with the control circuit element. As the control circuit element and MOS FET are on the same frame, this circuit also works for overheat in MOS FET.

### 3-2-8. Overvoltage Protection Circuit

This circuit actuates the latch circuit when the $V_{IN}$ terminal voltage exceeds 28.0V (minimum). Basically, this circuit operates as a $V_{IN}$ terminal overvoltage protector in the control circuit. Usually, the $V_{IN}$ terminal is supplied from the auxiliary winding of the transformer and this voltage is proportional to the output voltage, and these circuit works also for overvoltage of the secondary side output such as when the control circuit opens. In this case, the secondary side output voltage Vout at overvoltage protection is expressed by the equation:

$$Vout\ (OVP) = \frac{\textit{Supply voltage 28.0V(MIN) with OVP operating}}{\textit{$V_{IN}$ terminal voltage at normal operating}}$$

Another overvoltage protection circuit is provided on the +148V line and +15V line on the secondary side.

### 3-2-9. Relay SR85

The relay SR85 is used to make a short-circuit to minimize the power loss by the rash current limiting resistors R815 and R816 when the power is turned on. When the +15V line/+7V–1 line in the POWER-1 power supply output line is booted, the relay SR85 shorts the circuit.

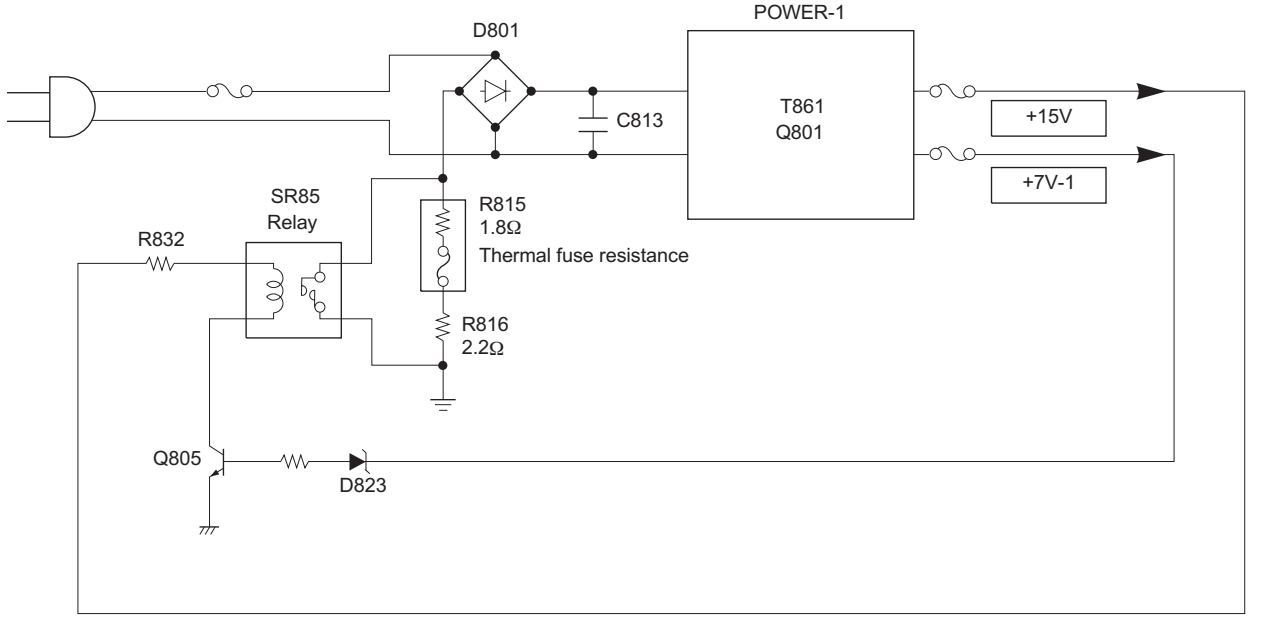


**Fig. 14-19**

# 4. POWER-2

## 4-1. Outline of Current Resonant Type Supply

Basic configuration of current resonant type power supply is shown on Fig. 14-20. Basic operation is as follow. Primary winding of converter trans and resonant capacitor are connected in series to consist of LC series resonant circuit. And this is drived by push-pull of two power MOS FET's.

Converter transformer operates in forward mode. Just when primary switching device turns ON, converter trans produces the secondary output.

Automatic voltage control operation is done in such way that +B voltage is detected by error amp. to be fed back to the primary OSC circuit via photo coupler, then controls frequency.

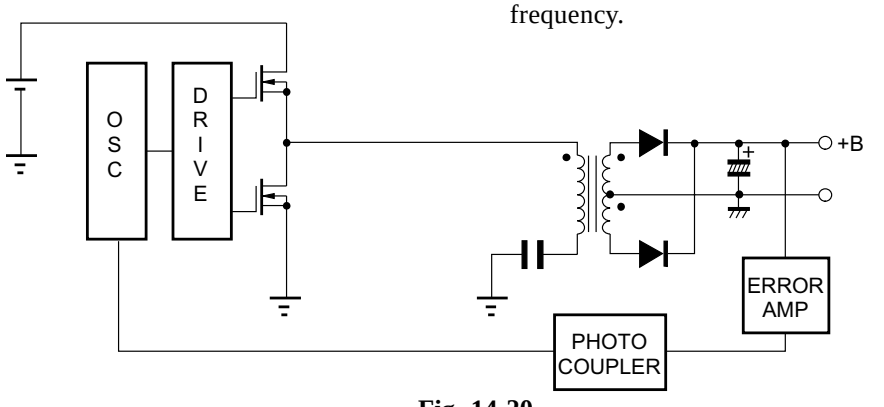


**Fig. 14-20**

## 4-2. Fundamental Theory

Voltage generating on L of LC series resonant circuit has characteristic which varies with frequency peaking at resonant point f= 1(2pÖLC) [Hz] as shown in Fig. 14-21. The circuit utilizes this characteristic to control output voltage. Actual operation is done at higher frequency than resonant point. By this operation, variable range of voltage across L ranges from maximum voltage of resonant point to power line voltage.

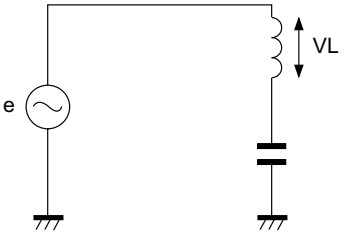


**Fig. 14-21**

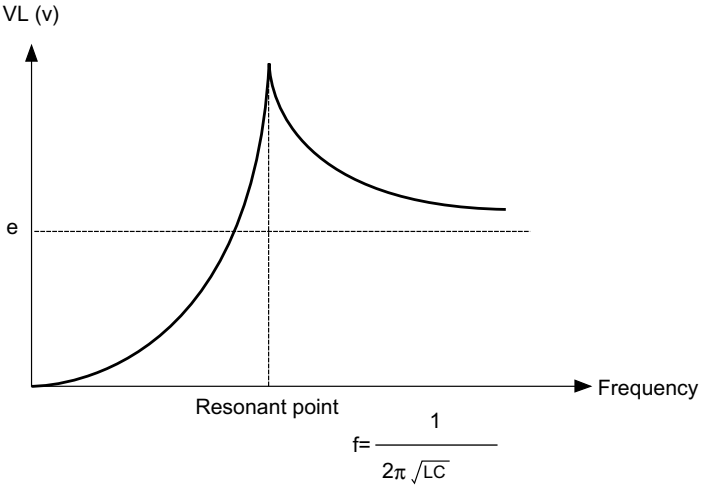


**Fig. 14-22**

## 4-3. Actual Circuit

Two MOS FET's, driver which drives FET's and frequency control IC are combined inside HIC (Q888).

Converter transformer T888 is designed to have loose coupling between the primary and the secondary, and to have some extent of leakage inductance. This is the reason why L and C (leakage inductance and resonant capacitor) are resonated during period that rectifying circuit (diode) connected to the secondary winding conducts. Rectifying circuit of the secondary winding uses double wave rectifier considering current balance of switching device, because converter transformer is driven in push-pull. The function of STR-Z4151 is explained below. Fig. 14-23 shows block diagram and Fig. 14-24 shows waveforms.

**Table 14-2**

| Pin No. | Function |
|---|---|
| 1 | Half bridge power supply input |
| 2 | Control unit ground |
| 3 | Dead time determining resistor connection terminal |
| 4 | Oscillator capacitor connection terminal |
| 5 | Oscillator control terminal |
| 6 | Maximum frequency determining resistor connecting terminal |
| 7 | Soft start capacitor connecting terminal |
| 8 | Delay latch capacitor connecting terminal |
| 9 | Control unit power supply terminal |
| 10 | Gate drive circuit power supply output |
| 11 | Out-of-resonance/overcurrent detection terminal |
| 12 | Half bridge GND |
| 14 | Half bridge output |
| 15 | High side gate drive power supply input |

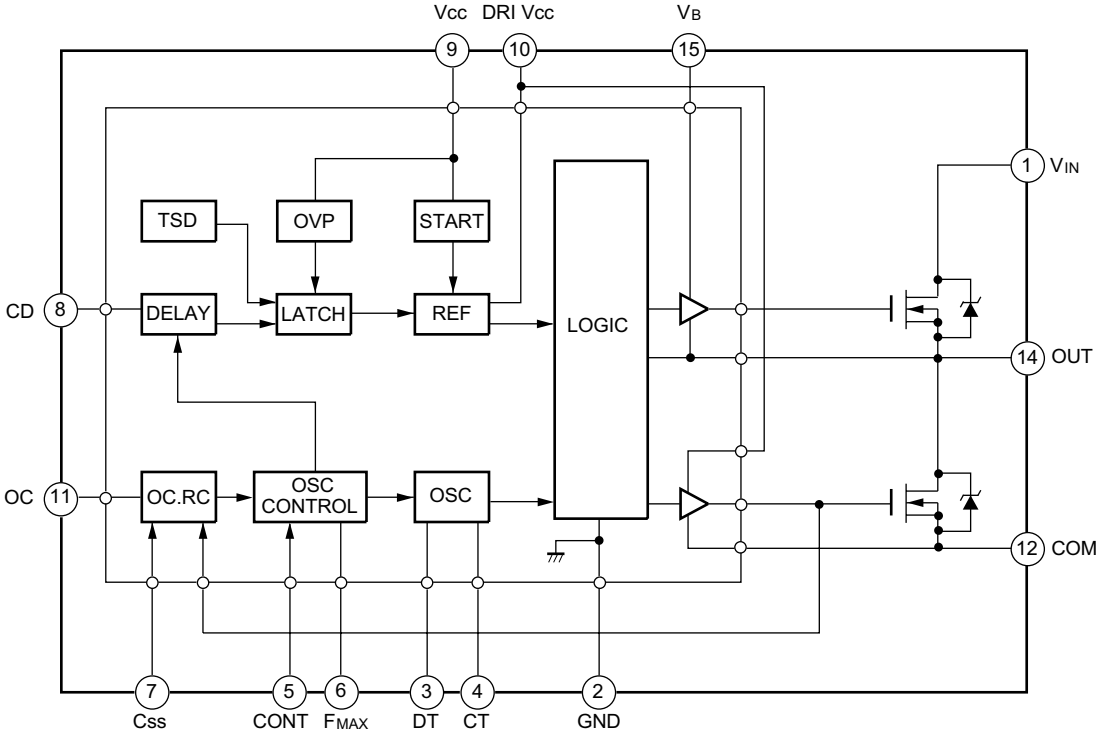


**Fig. 14-23 STR-Z4151**

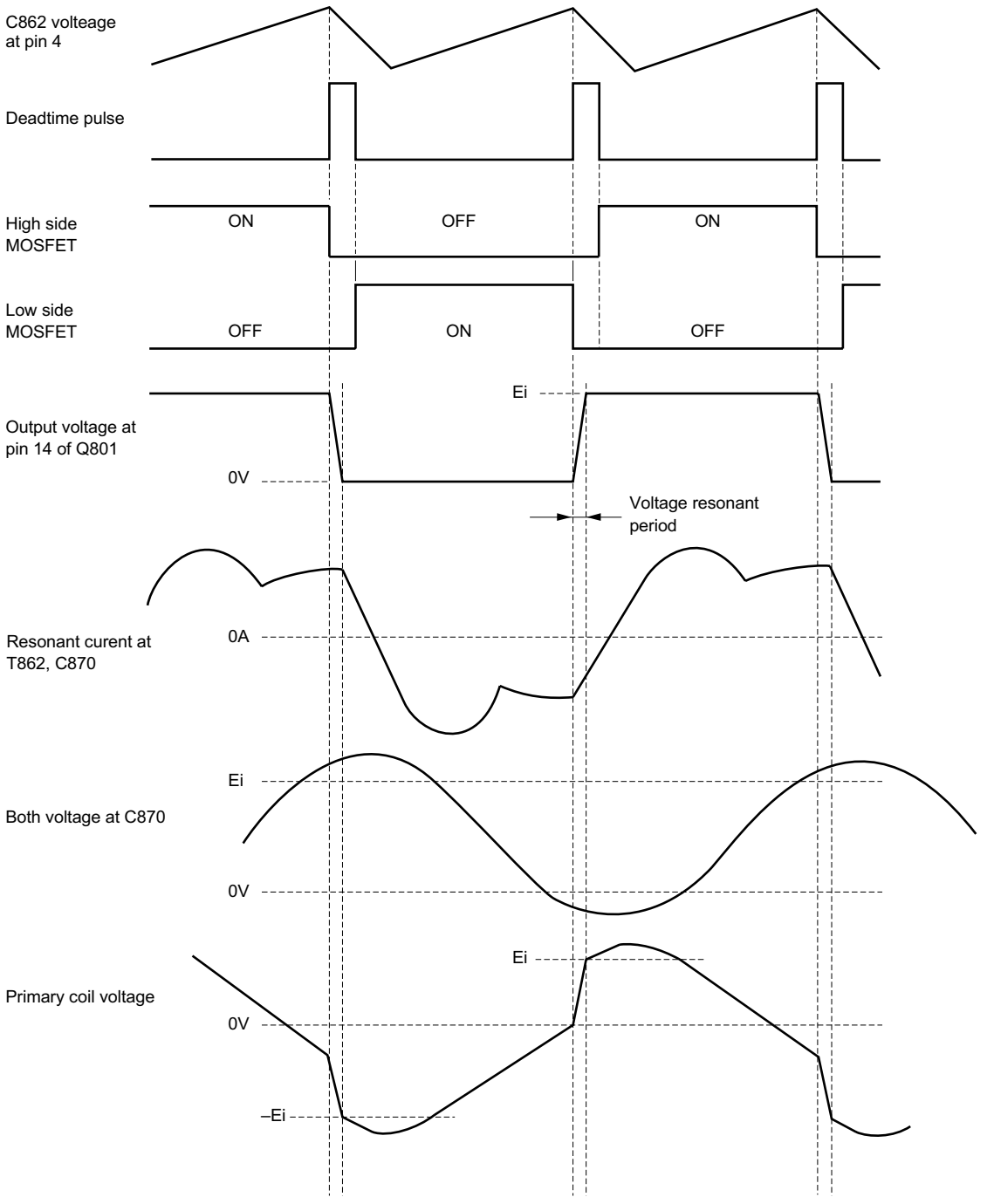
C862 volteage at pin 4
Deadtime pulse
High side MOSFET
ON
OFF
ON
Low side MOSFET
OFF
ON
OFF
Ei
Output voltage at pin 14 of Q801
0V
Voltage resonant period
Resonant curent at T862, C870
0A
Ei
Both voltage at C870
0V
Ei
Primary coil voltage
0V
–Ei

**Fig. 14-24**

## 4-4. Main Functions of the Control Unit

### 4-4-1. Oscillator (OSC)

**(1) Main oscillator**

The charge/discharge time of the capacitor C862 (680 pF) connected to the CT terminal (pin 4) determines the ON time of the high/low sides power MOSFET. The threshold level of charging/discharging the capacitor is about 1.8V and 2.7V. The charge-to-discharge ratio is fixed to about 3:1. The minimum oscillation frequency of the main oscillator is set to about 25 kHz by the time constant in the IC.

**(2) Dead time oscillator**

This determines the dead time period for resonating the voltage by turning off the high/low sides power MOSFET at the ON/OFF timing. The dead time is determined by the capacitor in the IC and the resistor R867 connected to the DT terminal (pin 3).

### 4-4-2. Control of the Main Oscillator

The main oscillator frequency is controlled by the following three terminal functions.

**(1) Fmax terminal (pin 6)**

The maximum frequency of the main oscillator and the output current of the Css terminal (pin 7) are determined by the output current of the resistor R868 connected to this terminal.

**(2) Css terminal (pin 7)**

The capacitor C866 is connected to this terminal to make the soft start function. At startup, this capacitor is charged with the current determined by the resistor R868 connected to the Fmax terminal (pin 6). The main oscillator frequency is lowered gradually from the maximum value. When the operation stops, the charged capacity is discharged with the internal circuit.

**(3) CONT terminal (pin 5)**

The main oscillator frequency changes with the output current of this terminal. When the output current rises over 200 µA, the main oscillator frequency increases. When the output current is lower than 200 µA, the delay latch circuit is activates. The output current does not increases higher than the maximum frequency determined by R868. If the output current rises over 3.4 mA, the main oscillator stops and both high and low sides power MOSFETs turn off.

### 4-4-3. Delay latch function

This shuts down the output (both high and low sides MOSFETs turn off) in the following conditions, and holds the state.

**(1) The output current of the CONT terminal decreases lower than 200 µA.**

This condition always occurs at start and stop of operation, and the operation is latched after a certain delay time. The delay time is determined by the charging time of the capacitor C869 connected to the CD terminal (pin 8). When the output current of the CONT terminal is higher than 200 µA, the CD terminal voltage is clamped to about 0.37V with the IC internal circuit. When the output current of the CONT terminal is lower than 200 µA, the clamp is reset and the CD terminal outputs a constant current of 6.3 µA to charge C869. When the CD terminal voltage rises to about 4.3V, the latch circuit operates and shuts down the output, and at the same time the IC internal circuit rapidly charges the CD terminal to about 5.7V, holding the latch mode.

(2) The Vcc terminal (pin 9) voltage exceeds 24V (overvoltage protection function) or the control IC junction temperature exceeds 150°C (thermal shutdown function).

C869 is rapidly charged with the IC internal circuit to shut down the output almost momentary. The holding after shutdown is the same as (1). To reset the latch mode, decrease the Vcc terminal voltage to the operation stop voltage (approx. 7.6V) or lower or decrease the CD terminal voltage to 4.3V or lower. In the TF71G90, reset by disconnecting the AC power cord.

#### 4-4-4. Overcurrent protection of the resonance circuit

The resonance circuit current is limited by increasing the main oscillator frequency. When overcurrent is detected, the current of C866 is disconnected from the Css terminal (pin 7), the voltage at the Css terminal is lowered and the main oscillator frequency is increased to protect the circuit against overcurrent. The following two steps of operation is performed according to the input voltage level at the OC terminal (pin 11).

**(1) OC (Low) threshold voltage: +1.8V (typ)**

Only when the input voltage at the OC terminal is higher than +1.8V (type), disconnect the current of C866 from the Css terminal, decrease gradually the Css terminal voltage and increase gradually the main oscillator frequency. Continue this operation until the OC terminal voltage decreases to +1.8V or lower.

**(2) OC (High) threshold voltage: +2.5V (typ)**

When the input voltage at the OC terminal exceeds +2.5V (typ), the IN internal circuit increases momentary the main oscillator frequency to Fmax and at the same time discharges C866 rapidly. When the Css terminal voltage decreases to 0.7V or lower, the circuit is reset and C866 is charged again. The main oscillator frequency decreases gradually as a result. If an overcurrent continues due to a defective part, the delay latch operates and oscillation stops.

#### 4-4-5. Restoration from Out-of-resonance

Out-of-resonance is detected by the OC terminal input signal and the gate drive signal of the low side power MOSFET. At the timing when the OC terminal input signal turns from negative to positive, existence of the gate drive signal is detected at the point of crossing -0.1V (type). If the gate drive signal exists, the resonance circuit is judged out of resonance. C866 is discharged and the main oscillator frequency is increased to restore the out-of-resonance. This operation continues until the resonance circuit regains normal operation.

Fig. 14-25 shows a detection of out of resonace waveform

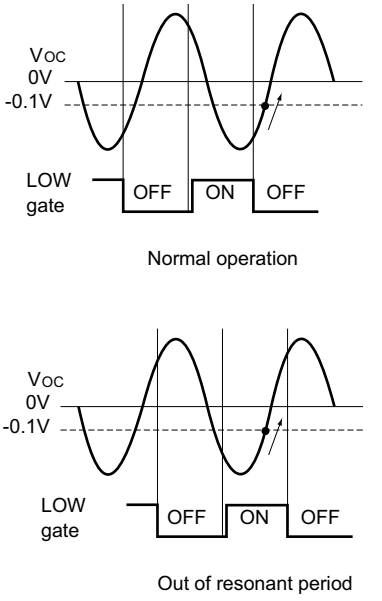


**Fig. 14-25 Detection of out-of-resonance**

#### 4-4-6. Constant Voltage Power Supply for the High Side Power MOSFET Gate Drive Circuit

Constant 8V is generated at the DRI terminal (pin 10), and is applied to the VB terminal (pin 15) as a power supply for the gate drive of the high side power MOSFET through the boot strap circuit (C863, C873, R862, D862). As a power supply for the gate drive of the low side power MOSFET, 8V is generated within the IC.

# 5. PROTECT FUNCTION

When the power voltage (OVP) and power current (OCP) in the DEF, CONV and power supply circuits are abnormal, the protect function works to protect flowing the power current.

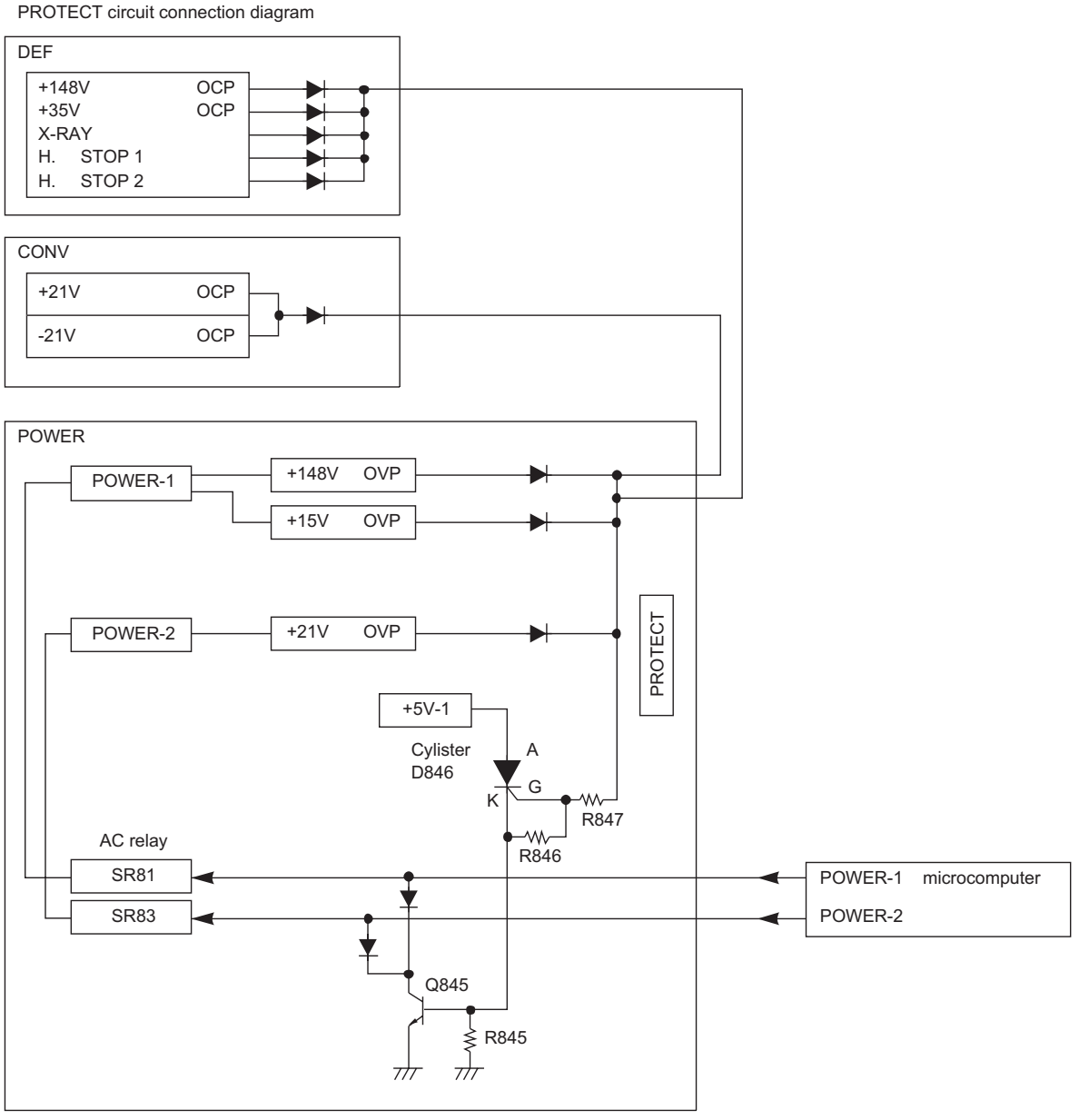


**Fig. 14-26 Protection circuit connection diagram**

- When the protect signal develops higher than 0.825V (MIN), D846 cylister is latched with ON status and Q845 turns ON.
- POWER-1 and POWER-2 signals becomes L level.
- SR81 and SR82 (AC relay) turn OFF.
- AC power supply current stops flowing to the POWER-1 and POWER-2 circuits.
- The status described right is not released until the power plug is pulled out.

# 6. TROUBLESHOOTING

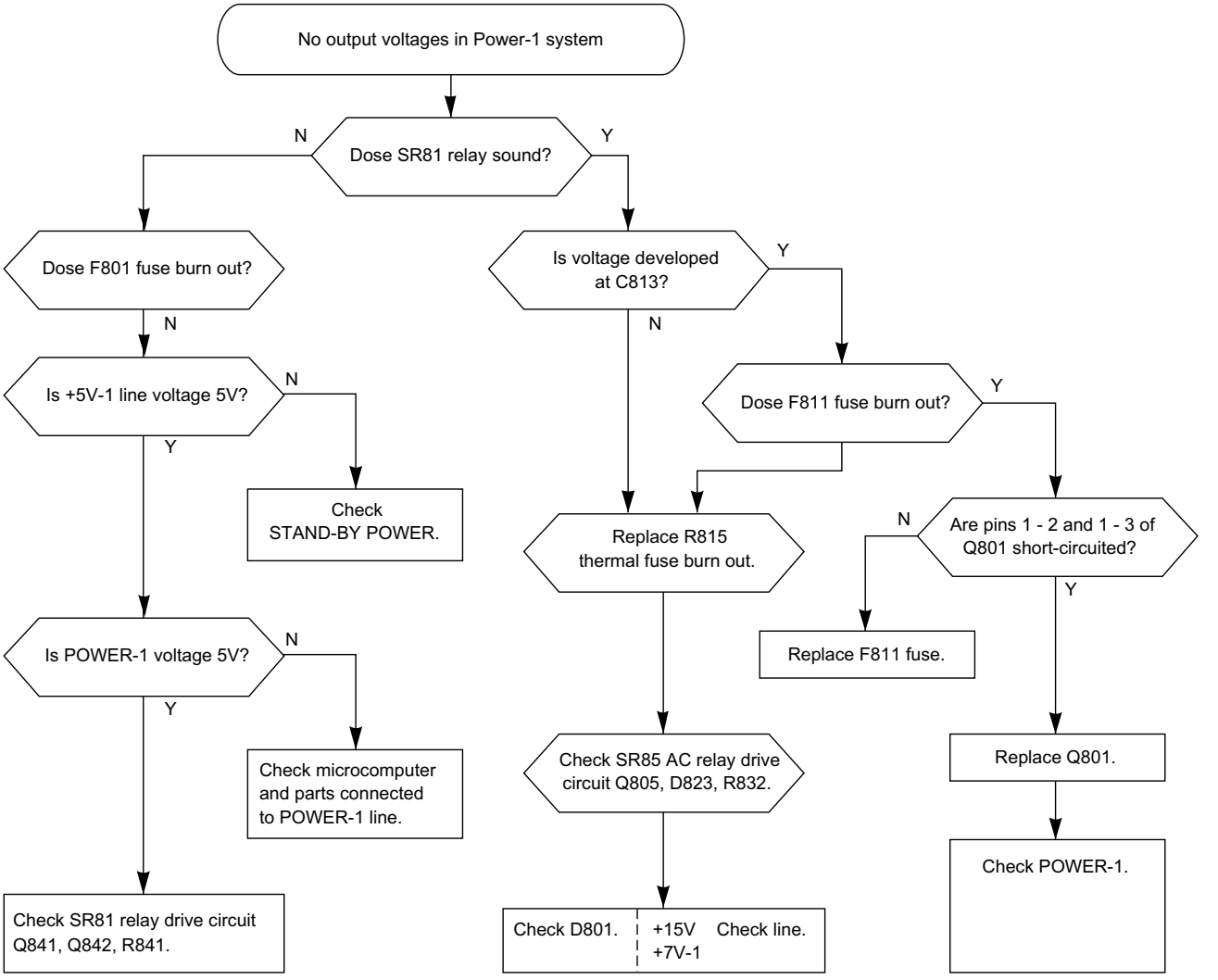


**Fig. 14-27**

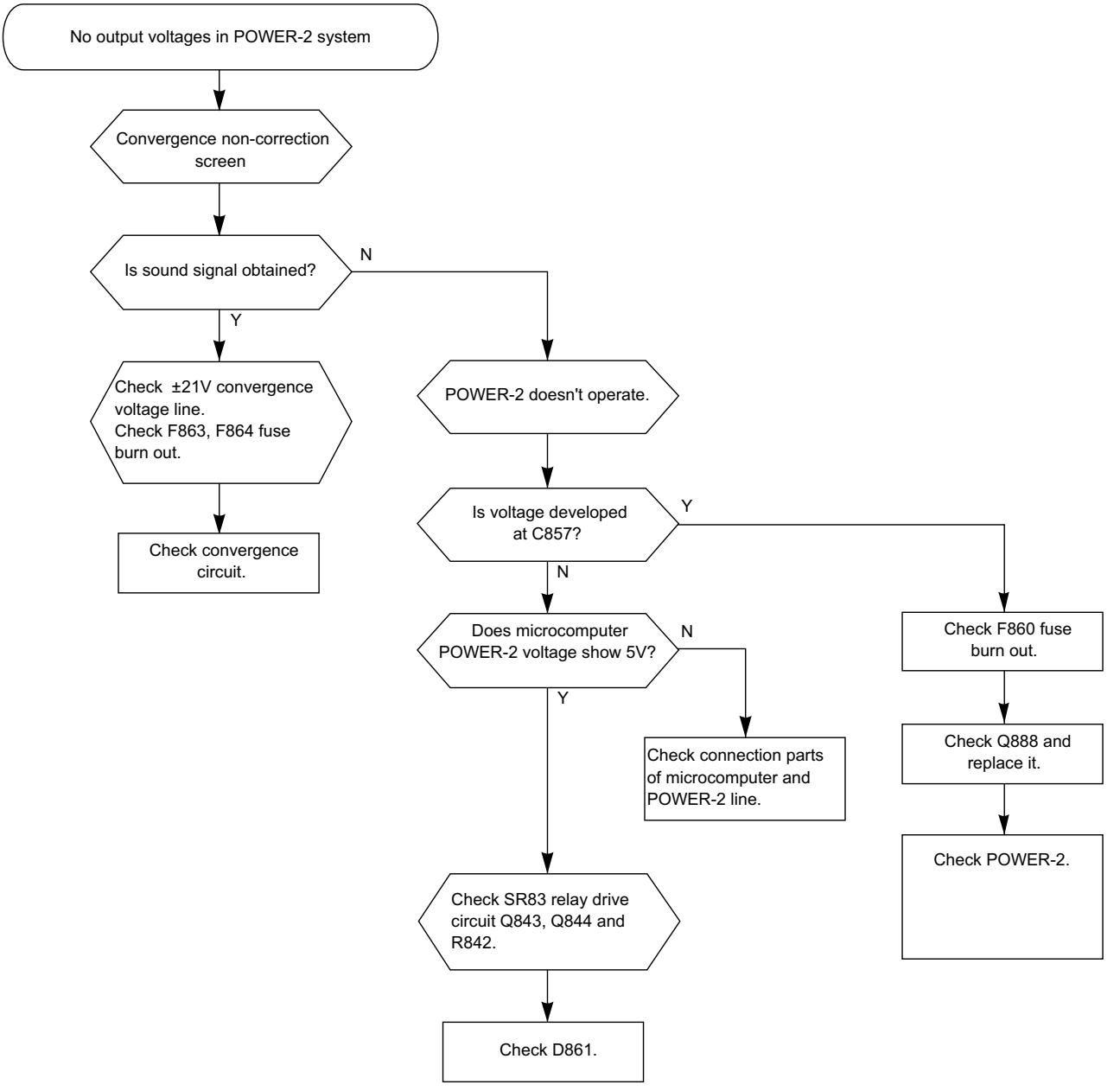
No output voltages in POWER-2 system
Convergence non-correction screen
Is sound signal obtained?
N
Y
Check ±21V convergence voltage line.
Check F863, F864 fuse burn out.
Check convergence circuit.
POWER-2 doesn't operate.
Is voltage developed at C857?
Y
N
Does microcomputer POWER-2 voltage show 5V?
N
Y
Check connection parts of microcomputer and POWER-2 line.
Check SR83 relay drive circuit Q843, Q844 and R842.
Check D861.
Check F860 fuse burn out.
Check Q888 and replace it.
Check POWER-2.

**Fig. 14-28**

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# SECTION XV
# CLOSED CAPTION/EDS CIRCUIT

# 1. OUTLINE

CC circuit extracts data of CC (Closed Caption) from input video signal, and decode them to generate display signal. Major feature of CC circuit of TG1-C chassis is as follow.

(1) Employing 1 chip decoder of stand alone type

(2) Acceptable of field 2 data ( CAPTION 3, 4 TEXT 1, 2) as well as field 1 data ( CAPTION 1, 2 TEXT 1, 2)

(3) Display of text mode extends from 8 rows to 15 rows.

(4) Extended character display of 64 kinds standing for Spanish and the like.

(5) Representing Background attributes (8 colors + transparent)

# 2. DATA TRANSMISSION FORMAT

CC data is transmitted being superimposed on line 21, field 1 (21H) and field 2 (284H). Waveform of line 21 is shown in Fig. 15-1. Line 21 signal is composed of data of 7 cycle clock-run-in, start bit and 16 bit (8bits x 2 bytes).

# 3. DISPLAY FORMAT

Character display area of caption mode and text mode consists of 32 characters x 15 rows as shown in Fig. 15-2.

On front and back of each row, 1 character blank area is respectively added. In caption mode, up to 8 rows among 15 rows can be displayed at the same time. Characters in text mode are displayed in black box of 34 characters x 15 rows.

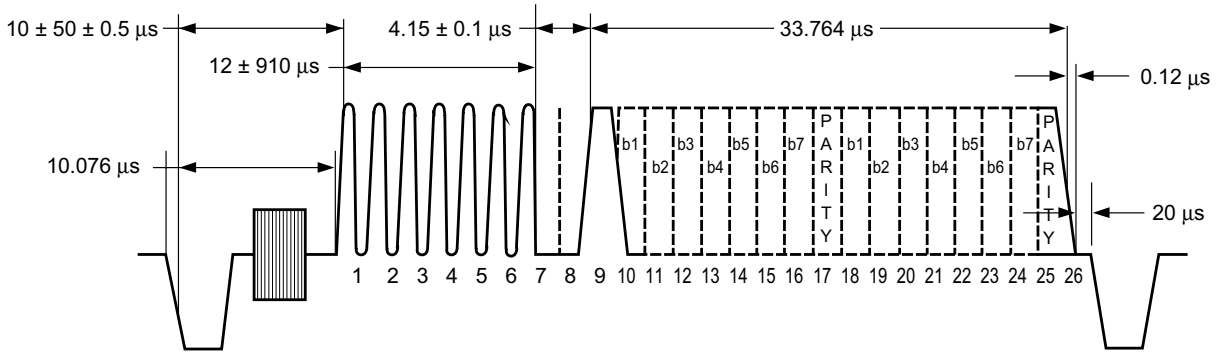


**Fig. 15-1**

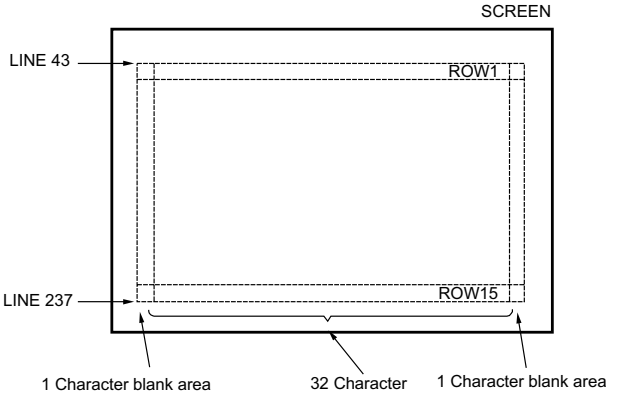


**Fig. 15-2**

# 4. CIRCUIT OPERATION

Block diagram of CC circuit is shown in Fig. 15-4.

Video signal which is input to pin 9 of UM01 is changed to 1 V(p-p) signal which is band-limited to 600 kHz by the input circuit, and it is supplied to pin 22 of QM01.

Inside QA01, line 21 signal is extracted from input video signal, and is recovered on clock and data. Recovered data is decoded by command processor and converted to display signal of R, G, B, Ys in Output Logic section.

The display signal is output at pins 52, 51, 50 and 49 in the CMOS level of positive polarity. The RGB output is sent to V/C/D IC and the screen is displayed.

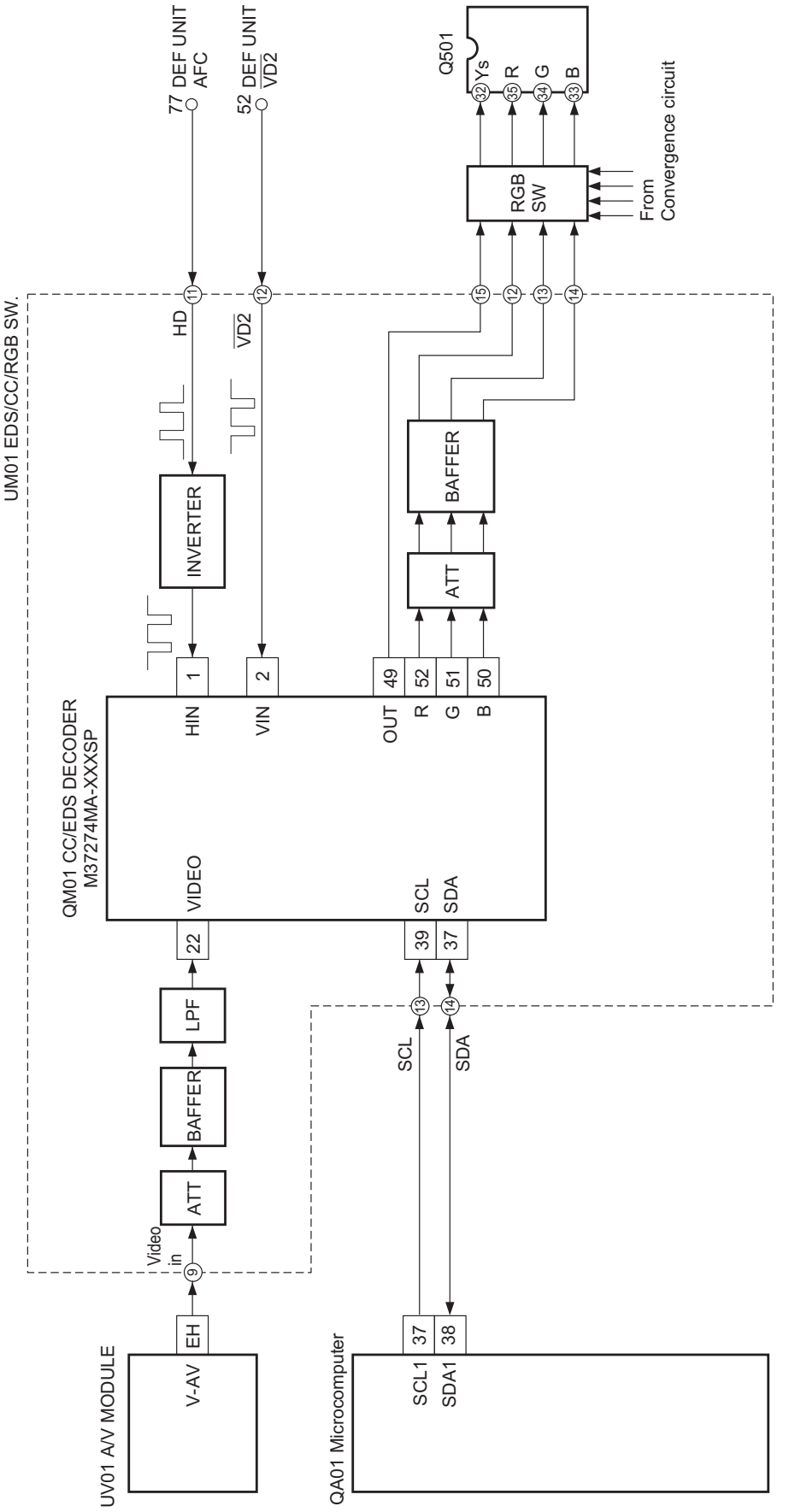
UM01 EDS/CC/RGB SW.
77 DEF UNIT AFC
52 DEF UNIT VD2
Q501
Ys
R
G
B
RGB SW
From Convergence circuit
HD
VD2
INVERTER
BAFFER
ATT
QM01 CC/EDS DECODER M37274MA-XXXSP
HIN
VIN
OUT
R
G
B
VIDEO
SCL
SDA
LPF
BAFFER
ATT
Video in
EH
V-AV
UV01 A/V MODULE
SCL1
SDA1
QA01 Microcomputer

**Fig. 15-3**

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